1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM,MLB,M82

MACBOOK AIR (JAN 2007)

PRODUCTION

01/25/2009

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
J		667176	PRODUCTION RELEASED	01/25/09	

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72 108	M82 Power and Ground Nets	(MASTER) (MASTER)
73 109	M82 Rule Definitions	(MASTER) (MASTER)

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7230	1	SCHEM,MLB,M82	SCH	CRITICAL	
820-2179	1	PCBF,MLB,M82	PCB	CRITICAL	

DRAWING
TITLE=M82_MLB
ABBREV=DRAWING
LAST_MODIFIED=Sun Jan 25 09:33:52 2009

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH
NOTED AS
APPLICABLE

SIZE D

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TITLE
SCHEM,MLB,M82

DRAWING NUMBER 051-7230
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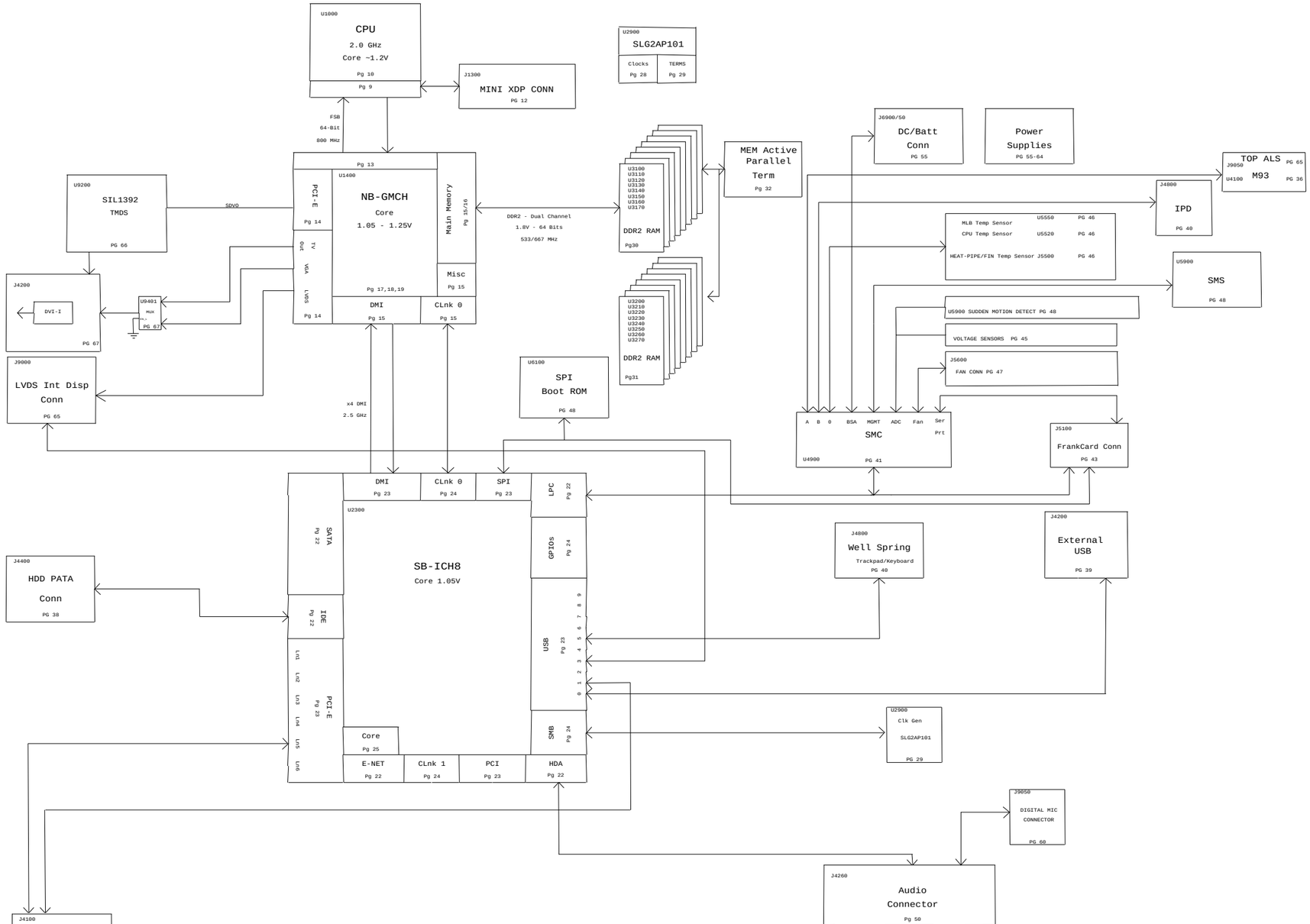

System Block Diagram

SYNC_MASTER=WFERRY-WF SYNC_DATE=05/11/2006

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SCALE	SHT	OF
NONE	2	109

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M82 POWER SYSTEM ARCHITECTURE

AC ADAPTER IN — J6980 — PP18V5_DCIN — 6A FUSE F6900 — =PP18V5_G3H_CHGR

=PPDCIN_G3H, PPVBAT_G3H_R, PPBUSB_G3H — D6901 ×3 — =PPDCIN_G3H

ENABLE — 3.425V G3HOT — LT1934 — U7790 — (PAGE 62) — PP3V42_G3H_REG (? A MAX CURRENT)

PP3V42_G3H_SMC — SMC PWRGD — RN5VD30A-F — U5000 — (PAGE 41) — SMC_RESET_L

SMC_BATT_CHG_EN

ENABLES — VOUT — PBUS CONVERTER/ BATTERY CHARGER — ISL6258 — U7900 — VIN — (PAGE 63) — CHGR_SMBUS

PPVBAT_G3H_CHGR_REG — 7A FUSE — PPBUSB_G3H — R7980 — =PBUSA_G3H

BATTERY 2S2P

Q7950 — R7930 — CHGR_BGATE — BATT_POS_F

VIN — 1.05V — ENA1 — VOUT1 — PP1V05_S0_REG (9.9 A MAX CURRENT)
1V05S0_RUNSS (S0)

1.5V — ENA2 — VOUT2 — PP1V5_S0_REG (3.3 A MAX CURRENT)
1V5S0_RUNSS (S0)

TPS51124 — U7300 — (PAGE 58) — PGOOD_1V5S0 — PGOOD_1V05S0

CLOCK — SLG2AP101 — U2900 — (PAGE 28) — CLK_PWRGD — PWRGD

NB_RESET_L, TMDS_RST_L, AIRPORT_RST_L, LCDBKLT_PLT_RST_L

ICH8M — CK_PWRGD — VRMPWRGD — PWRBTN* — PLTRST* — RSMRST* — PWROK — CPU_PWRGD(GPIO49) — U2300 — (PAGE 22)

U2803 — VR_PWRGD_CK505 — VR_PWRGD_CLKEN

PLT_RST_L — U2880

PM_SB_PWROK — U2801 — CPU_PWRGD

CPU — PWRGOOD — RESET* — U1000 — (PAGE 9)

CRESTLINE — PWROK — H_CPURST* — FSB_CPURST_L — U1400 — (PAGE 13)

Q7860 — DELAY R-10K C-0.002uF P5VS3_EN_L (S3) — DELAY R-10K C-0.01uF P3V3S3_EN_L (S3)

CPUVCORE — VIN — VOUT — CLKEN# — VR_ON — PGOOD — ISL6261CRZ — U7100 — (PAGE 56)
IMVP_VR_ON — PPVCORE_S0_CPU_REG — PPVCORE_S0_CPU (30 A MAX CURRENT)
VR_PWRGD_CK505_L — VR_PWRGOOD_DELAY

ICH — PM_S4_STATE_L — PM_SLP_S3_L

SMC — PG2 PG3 — U4900 P60 — (PAGE 40) — SMC_PM_G2_EN (S5)

PPBUS_G3H — =PPBUSB_G3H

Q7000 — P5VS0_EN — PP5V_S0 — TPS79933 — U2280 — (PAGE 21) — P3V3_S0_NB_TVDAC (205mA MAX CURRENT)

Q7865 — P5VS3_EN_L — PP5V_S3

5V — EN1 — VO1 — PP5V_S5_REG (? A MAX CURRENT) — PP5V_S5
3.3V — EN2 — VO2 — PP3V3_S5_REG (? A MAX CURRENT) — PP3V3_S5
5VS5_RUNSS (S5)
3VS5_RUNSS (S5)
TPS51120 — U7600 — (PAGE 60) — PGOOD1,2 — RSMRST_PWRGD

Q7866 — P3V3S3_EN_L — PP3V3_S3 — 1V25S0_RUNSS — 1.25V S0 — EN — LTC3412A — U7750 — VIN — VOUT — (PAGE 61) — PP1V25_S0_REG (3 A MAX CURRENT)

Q7001 — P3V3S0_EN — PP3V3_S0

U7002 — PP1V25_S0_FET — ALL_SYS_PWRGD_AND — PGOOD_1V5S0 — PGOOD_1V05S0 — PGOOD_SEQUENCER

SMC — RSMRST_OUT(P15) — PWRGD(P12) 99ms DLY — IMVP_VR_ON(P16) — RSMRST_IN(P13) — PLT_RST* — PWR_BUTTON(P90) — P17(BTN_OUT) — RST* — SLP_S5_L(P95) — SLP_S4_L(P94) — SLP_S3_L(P93) — U4900 — (PAGE 40)
PM_RSMRST_L, IMVP_VR_ON, SMC_LRESET_L, PM_PWRBTN_L, SMC_RESET_L
SMC_ONOFF_L — BATTERY ONLY: 05 — ADAPTER IN : 10-1

SMC_ADAPTER_PRESENT — WOW_EN — PM_WLAN_EN_L

GPU_VCORE — VIN — VCC — EN — VOUT — ADP3209 — U7200 — (PAGE 57) — GFX_VR_EN — GCORE_EN — PP5V_S0_NB_GFX_IMVP — =PPVCORE_S0_NB_GFX_IMVP (13 A MAX CURRENT)

Q7004 — P1V8S0_EN — PP1V8_S3_FET — =PP1V8_S0_FET — =PP1V8_S0_NB_DPLL — MCH DPLL — TPS731125 — U2265 — (PAGE 21) — P1V25_S0_NB_DPLL

R7870 — 1V8S3_RUNSS — PM_SLP_S3_L — PP1V8_S3_REG

VIN — VLDOIN — S5 — 1.8V — VOUT1 — (11 A MAX CURRENT) — PP1V8_S3_REG
S3 — 0.9V — VOUT2 — PP0V9_S0_REG — PGOOD_1V8S3
TPS51116 — U7500 — (PAGE 59)

RUNSS_GATE_D — Q7006 Q7007 DELAY R-330 C-0.022uF 1V5S0_RUNSS (S0)
Q7006 Q7007 DELAY R-330 C-0.01uF 1V05S0_RUNSS (S0)
Q7006 Q7006 DELAY R-330 C-1000PF 1V25S0_RUNSS (S0)

RST* — U7000 — GATE A — GATE B — GATE C — GATE D — ISL6130IRZA — (PAGE 56)
UVLO_A — UVLO_B — UVLO_C — UVLO)D — ENABLE_1
PGOOD_1V8S3 — PP5V_S0_FET — PP3V3_S0_FET — PP1V8_S0_FET — PM_SLP_S3_L
P5VS0_EN — P3V3S0_EN — P1V8S0_EN — RUNSS_GATE_D

Power Block Diagram

SYNC_MASTER=POWER — SYNC_DATE=06/30/2005

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BOMs

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7886	PCBA,MLB,1.6GHZ,MI 2GB,SS CAP,M82	EEE_XSC,M82_COMMON,M82_MICRON,CPU_PRQ_1_6GHZ,M82_SS_CAP
630-9024	PCBA,MLB,1.6GHZ,HY 2GB,SS CAP,M82	EEE_YMS,M82_COMMON,M82_HYNIX,CPU_PRQ_1_6GHZ,M82_SS_CAP
630-9133	PCBA,MLB,1.8GHZ,MI 2GB,SS CAP,M82	EEE_Z80,M82_COMMON,M82_MICRON,CPU_PRQ_1_8GHZ,M82_SS_CAP
630-9134	PCBA,MLB,1.8GHZ,HY 2GB,SS CAP,M82	EEE_Z81,M82_COMMON,M82_HYNIX,CPU_PRQ_1_8GHZ,M82_SS_CAP
630-9204	PCBA,MLB,1.6GHZ,HY 2GB,MU CAP,M82	EEE_ZU5,M82_COMMON,M82_HYNIX,CPU_PRQ_1_6GHZ,M82_MU_CAP
630-9205	PCBA,MLB,1.6GHZ,HY 2GB,TY CAP,M82	EEE_ZU6,M82_COMMON,M82_HYNIX,CPU_PRQ_1_6GHZ,M82_TY_CAP
630-9206	PCBA,MLB,1.6GHZ,MI 2GB,MU CAP,M82	EEE_ZU7,M82_COMMON,M82_MICRON,CPU_PRQ_1_6GHZ,M82_MU_CAP
630-9207	PCBA,MLB,1.6GHZ,MI 2GB,TY CAP,M82	EEE_ZU8,M82_COMMON,M82_MICRON,CPU_PRQ_1_6GHZ,M82_TY_CAP
630-9208	PCBA,MLB,1.8GHZ,HY 2GB,MU CAP,M82	EEE_ZU9,M82_COMMON,M82_HYNIX,CPU_PRQ_1_8GHZ,M82_MU_CAP
630-9209	PCBA,MLB,1.8GHZ,HY 2GB,TY CAP,M82	EEE_ZUA,M82_COMMON,M82_HYNIX,CPU_PRQ_1_8GHZ,M82_TY_CAP
630-9210	PCBA,MLB,1.8GHZ,MI 2GB,MU CAP,M82	EEE_ZUB,M82_COMMON,M82_MICRON,CPU_PRQ_1_8GHZ,M82_MU_CAP
630-9211	PCBA,MLB,1.8GHZ,MI 2GB,TY CAP,M82	EEE_ZUC,M82_COMMON,M82_MICRON,CPU_PRQ_1_8GHZ,M82_TY_CAP

Bar Code Label / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:XSC]	CRITICAL	EEE_XSC
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:YMS]	CRITICAL	EEE_YMS
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:Z80]	CRITICAL	EEE_Z80
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:Z81]	CRITICAL	EEE_Z81
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZU5]	CRITICAL	EEE_ZU5
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZU6]	CRITICAL	EEE_ZU6
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZU7]	CRITICAL	EEE_ZU7
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZU8]	CRITICAL	EEE_ZU8
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZU9]	CRITICAL	EEE_ZU9
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZUA]	CRITICAL	EEE_ZUA
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZUB]	CRITICAL	EEE_ZUB
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZUC]	CRITICAL	EEE_ZUC

BOMOPTION Groups

BOM GROUP	BOM OPTIONS
M82_COMMON	ALTERNATE,COMMON,M82_COMMON1,M82_COMMON2,M82_COMMON3
M82_COMMON1	ISL6258,BOOTROM_FINAL,SMC_PRGRM
M82_COMMON2	SMS_MOT_DIS,LPCPLUS,XDP,DRAM_2GB
M82_COMMON3	
M82_MICRON	DRAM_MICRON,DRAM_SPD_1
M82_HYNIX	DRAM_HYNIX,DRAM_SPD_2
M82_HYNIX_LP	DRAM_HYNIX_LP,DRAM_SPD_2
M82_SS_CAP	SS_CAP_1UF,SS_CAP_2_2UF,SS_CAP_10UF
M82_MU_CAP	MU_CAP_1UF,MU_CAP_2_2UF,MU_CAP_10UF
M82_TY_CAP	TY_CAP_1UF,TY_CAP_2_2UF,TY_CAP_10UF

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3522	1	IC,SANTAYNEZ,MEROM,1.6GHZ,ES,20W,956BGA	U1000	CRITICAL	CPU_1_6GHZ
337S3523	1	IC,SANTAYNEZ,MEROM,1.8GHZ,ES,20W,956BGA	U1000	CRITICAL	CPU_1_8GHZ
338S0514	1	IC,965GM,CRESTLINE,USFF BGA	U1400	CRITICAL	
338S0515	1	IC,ICH8M,USFF BGA	U2300	CRITICAL	
359S0130	1	LOW POWER CLOCK SYNTHESIZER,SLG2AP101,68PIN	U2900	CRITICAL	
335S0510	1	IC, 16MBIT 8-PIN SERIAL FLASH,VWQPN	U6100	CRITICAL	BOOTROM_BLANK_2MB
335S0509	1	IC, 32MBIT 8-PIN SERIAL FLASH, WSON8	U6100	CRITICAL	BOOTROM_BLANK_4MB
341S2111	1	IC,EFI,BOOTROM DEVELOPMENT (UNLOCKED),M82	U6100	CRITICAL	BOOTROM_DEVEL
341S2112	1	IC,EFI,BOOTROM FINAL (LOCKED),M82	U6100	CRITICAL	BOOTROM_FINAL
337S3477	1	SST89V54RD MICROCONTROLLER	U9300	CRITICAL	SST8051_BLANK
341S2173	1	IC,PRGM,SST SST89V54RD,UCNTRLR,M82	U9300	CRITICAL	SST8051_PRGRM
338S0422	1	IC,SMC,HS8/2117	U4900	CRITICAL	SMC_BLANK
341S2115	1	IC,PRGRM,SMC (NEW),M82	U4900	CRITICAL	SMC_PRGRM
333S0406	4	MICRON,DRAM,64M16,8x12.5	U3100,U3110,U3120,U3130	CRITICAL	DRAM_MICRON
333S0406	4	MICRON,DRAM,64M16,8x12.5	U3140,U3150,U3160,U3170	CRITICAL	DRAM_MICRON
333S0406	4	MICRON,DRAM,64M16,8x12.5	U3200,U3210,U3220,U3230	CRITICAL	DRAM_MICRON
333S0406	4	MICRON,DRAM,64M16,8x12.5	U3240,U3250,U3260,U3270	CRITICAL	DRAM_MICRON
333S0411	4	HYNIX,DRAM,64M16,8x13	U3100,U3110,U3120,U3130	CRITICAL	DRAM_HYNIX
333S0411	4	HYNIX,DRAM,64M16,8x13	U3140,U3150,U3160,U3170	CRITICAL	DRAM_HYNIX
333S0411	4	HYNIX,DRAM,64M16,8x13	U3200,U3210,U3220,U3230	CRITICAL	DRAM_HYNIX
333S0411	4	HYNIX,DRAM,64M16,8x13	U3240,U3250,U3260,U3270	CRITICAL	DRAM_HYNIX
333S0415	4	HYNIX,DRAM,64M16,8x13,LP	U3100,U3110,U3120,U3130	CRITICAL	DRAM_HYNIX_LP
333S0415	4	HYNIX,DRAM,64M16,8x13,LP	U3140,U3150,U3160,U3170	CRITICAL	DRAM_HYNIX_LP
333S0415	4	HYNIX,DRAM,64M16,8x13,LP	U3200,U3210,U3220,U3230	CRITICAL	DRAM_HYNIX_LP
333S0415	4	HYNIX,DRAM,64M16,8x13,LP	U3240,U3250,U3260,U3270	CRITICAL	DRAM_HYNIX_LP
353S1938	1	IC,ISL6258,REV2,BAT CHGR, 28P QFN	U7900	CRITICAL	ISL6258
197S0213	1	14.318MHZ XTAL, 2.5x2.0	Y9390	CRITICAL	SST8051_14MHZ
197S0231	1	20MHZ XTAL, 2.5x2.0	Y9390	CRITICAL	SST8051_20MHZ
197S0257	1	33MHZ XTAL, 2.5x2.0	Y9390	CRITICAL	SST8051_33MHZ
337S3563	1	IC,SANTAYNEZ,MEROM,1.6GHZ,PRQ,REV3,20W,956BGA	U1000	CRITICAL	CPU_PRQ_1_6GHZ
337S3564	1	IC,SANTAYNEZ,MEROM,1.8GHZ,PRQ,REV3,20W,956BGA	U1000	CRITICAL	CPU_PRQ_1_8GHZ

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
128S0093	128S0092	ALL	33UF 20% 16V DCASE	
376S0466	376S0410	ALL	Si4413 for Si4405	
740S0044	740S0028	ALL	0.5A OC FUSE	
104S0023	104S0018	ALL	1206 1/4W .002 OHM	
152S0684	152S0421	ALL	1.0UH,22A,10MOHM	
338S0616	338S0515	ALL	USFF PRQ ICH8M B2	

CONFIGURATION OPTIONS

SYNC_MASTER=(N/A) SYNC_DATE=(N/A)

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1UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0629	5	CAP, 1UF, 6.3V, 10%, 0402	C1001,C1002,C2102,C2331,C2170	CRITICAL	SS_CAP_1UF
138S0629	9	CAP, 1UF, 6.3V, 10%, 0402	C2200,C2330,C2400,C2703,C2801,C2900,C7000,C7100,C7101	CRITICAL	SS_CAP_1UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0628	5	CAP, 1UF, 6.3V, 10%, 0402	C1001,C1002,C2102,C2331,C2170	CRITICAL	MU_CAP_1UF
138S0628	9	CAP, 1UF, 6.3V, 10%, 0402	C2200,C2330,C2400,C2703,C2801,C2900,C7000,C7100,C7101	CRITICAL	MU_CAP_1UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0630	5	CAP, 1UF, 6.3V, 10%, 0402	C1001,C1002,C2102,C2331,C2170	CRITICAL	TY_CAP_1UF
138S0630	9	CAP, 1UF, 6.3V, 10%, 0402	C2200,C2330,C2400,C2703,C2801,C2900,C7000,C7100,C7101	CRITICAL	TY_CAP_1UF

2.2UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1140,C1141,C1142,C1143,C1144,C1145,C1146,C1147,C1148,C1149	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240,C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248,C1249	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1300,C1301,C1302,C1303,C1304,C1305,C1306,C1307	CRITICAL	SS_CAP_2_2UF
138S0632	6	CAP, 2.2UF, 6.3V, 20%, 0402	C2214,C2215,C2240,C2241,C2242,C2243	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8000,C8001,C8002,C8003,C8004,C8005,C8006,C8007,C8008,C8009	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8010,C8011,C8012,C8013,C8014,C8015,C8016,C8017,C8018,C8019	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8020,C8021,C8022,C8023,C8024,C8025,C8026,C8027,C8028,C8029	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8030,C8031,C8032,C8033,C8034,C8035,C8036,C8037,C8038,C8039	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8000,C8001,C8002,C8003,C8004,C8005,C8006,C8007,C8008,C8009	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C8000,C8001,C8002,C8003,C8004,C8005,C8006,C8007	CRITICAL	SS_CAP_2_2UF
138S0632	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1300,C1301,C1302,C1303,C1307,C1308,C1201,C1202,C1203,C1204,C1205,C1206	CRITICAL	SS_CAP_2_2UF
138S0632	3	CAP, 2.2UF, 6.3V, 20%, 0402	C1022,C1023,C1000	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C5400,C5401,C5402,C5405,C5410,C5411,C5412,C5413,C5415,C5416	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C5220,C5221,C5222,C5225,C5230,C5231,C5232,C5235,C5240,C5241	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C5142,C5143,C5145,C5240,C5560,C5161,C5051,C5056	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C5400,C5401,C5402,C5405,C5410,C5411,C5412,C5413,C5416,C5417	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C5020,C5021,C5022,C5025,C5030,C5031,C5032,C5035,C5040,C5041	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C5042,C5043,C5045,C5048,C5049,C5051,C5052,C5055	CRITICAL	SS_CAP_2_2UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1140,C1141,C1142,C1143,C1144,C1145,C1146,C1147,C1148,C1149	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240,C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248,C1249	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1300,C1301,C1302,C1303,C1304,C1305,C1306,C1307	CRITICAL	MU_CAP_2_2UF
138S0633	6	CAP, 2.2UF, 6.3V, 20%, 0402	C2214,C2215,C2240,C2241,C2242,C2243	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8000,C8001,C8002,C8003,C8004,C8005,C8006,C8007,C8008,C8009	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8010,C8011,C8012,C8013,C8014,C8015,C8016,C8017,C8018,C8019	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8020,C8021,C8022,C8023,C8024,C8025,C8026,C8027,C8028,C8029	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8030,C8031,C8032,C8033,C8034,C8035,C8036,C8037,C8038,C8039	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8000,C8001,C8002,C8003,C8004,C8005,C8006,C8007,C8008,C8009	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C8000,C8001,C8002,C8003,C8004,C8005,C8006,C8007	CRITICAL	MU_CAP_2_2UF
138S0633	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1300,C1301,C1302,C1303,C1307,C1308,C1201,C1202,C1203,C1204,C1205,C1206	CRITICAL	MU_CAP_2_2UF
138S0633	3	CAP, 2.2UF, 6.3V, 20%, 0402	C1022,C1023,C1000	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C5400,C5401,C5402,C5405,C5410,C5411,C5412,C5413,C5415,C5416	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C5220,C5221,C5222,C5225,C5230,C5231,C5232,C5235,C5240,C5241	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C5142,C5143,C5145,C5240,C5560,C5161,C5051,C5056	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C5400,C5401,C5402,C5405,C5410,C5411,C5412,C5413,C5415,C5416	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C5020,C5021,C5022,C5025,C5030,C5031,C5032,C5035,C5040,C5041	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C5042,C5043,C5045,C5048,C5049,C5051,C5052,C5055	CRITICAL	MU_CAP_2_2UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1140,C1141,C1142,C1143,C1144,C1145,C1146,C1147,C1148,C1149	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240,C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248,C1249	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1300,C1301,C1302,C1303,C1304,C1305,C1306,C1307	CRITICAL	TY_CAP_2_2UF
138S0634	6	CAP, 2.2UF, 6.3V, 20%, 0402	C2214,C2215,C2240,C2241,C2242,C2243	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8000,C8001,C8002,C8003,C8004,C8005,C8006,C8007,C8008,C8009	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8010,C8011,C8012,C8013,C8014,C8015,C8016,C8017,C8018,C8019	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8020,C8021,C8022,C8023,C8024,C8025,C8026,C8027,C8028,C8029	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8030,C8031,C8032,C8033,C8034,C8035,C8036,C8037,C8038,C8039	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8000,C8001,C8002,C8003,C8004,C8005,C8006,C8007,C8008,C8009	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C8000,C8001,C8002,C8003,C8004,C8005,C8006,C8007	CRITICAL	TY_CAP_2_2UF
138S0634	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1300,C1301,C1302,C1303,C1307,C1308,C1201,C1202,C1203,C1204,C1205,C1206	CRITICAL	TY_CAP_2_2UF
138S0634	3	CAP, 2.2UF, 6.3V, 20%, 0402	C1022,C1023,C1000	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C5400,C5401,C5402,C5405,C5410,C5411,C5412,C5413,C5415,C5416	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C5220,C5221,C5222,C5225,C5230,C5231,C5232,C5235,C5240,C5241	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C5142,C5143,C5145,C5240,C5560,C5161,C5051,C5056	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C5400,C5401,C5402,C5405,C5410,C5411,C5412,C5413,C5415,C5416	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C5020,C5021,C5022,C5025,C5030,C5031,C5032,C5035,C5040,C5041	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C5042,C5043,C5045,C5048,C5049,C5051,C5052,C5055	CRITICAL	TY_CAP_2_2UF

10UF 0603 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0626	10	CAP, 10UF, 6.3V, 20%, 0603	C1300,C1301,C1302,C1303,C1304,C1305,C1306,C1307,C1308,C1309	CRITICAL	SS_CAP_10UF
138S0626	10	CAP, 10UF, 6.3V, 20%, 0603	C1210,C1211,C1212,C1213,C1214,C1215,C1216,C1217,C1218,C1219	CRITICAL	SS_CAP_10UF
138S0626	10	CAP, 10UF, 6.3V, 20%, 0603	C1220,C1221,C1222,C1223,C1224,C1225,C1226,C1227,C1228,C1229	CRITICAL	SS_CAP_10UF
138S0626	3	CAP, 10UF, 6.3V, 20%, 0603	C1230,C1231,C1300	CRITICAL	SS_CAP_10UF
138S0626	9	CAP, 10UF, 6.3V, 20%, 0603	C2100,C2101,C2212,C2219,C2221,C2232,C2260,C2261,C2262	CRITICAL	SS_CAP_10UF
138S0626	5	CAP, 10UF, 6.3V, 20%, 0603	C2701,C2700,C2708,C2720,C2901	CRITICAL	SS_CAP_10UF
138S0626	6	CAP, 10UF, 6.3V, 20%, 0603	C5200,C5201,C5202,C5500,C5501,C5502	CRITICAL	SS_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	C4100,C4400,C4613,C5000,C7201,C7301,C7350,C7351	CRITICAL	SS_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	C7502,C7507,C7600,C7641,C7803,C7804,C7900,C7909	CRITICAL	SS_CAP_10UF
138S0626	5	CAP, 10UF, 6.3V, 20%, 0603	C8012,C8201,C8205,C8213,C8218	CRITICAL	SS_CAP_10UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0625	10	CAP, 10UF, 6.3V, 20%, 0603	C1300,C1301,C1302,C1303,C1304,C1305,C1306,C1307,C1308,C1309	CRITICAL	MU_CAP_10UF
138S0625	10	CAP, 10UF, 6.3V, 20%, 0603	C1210,C1211,C1212,C1213,C1214,C1215,C1216,C1217,C1218,C1219	CRITICAL	MU_CAP_10UF
138S0625	10	CAP, 10UF, 6.3V, 20%, 0603	C1220,C1221,C1222,C1223,C1224,C1225,C1226,C1227,C1228,C1229	CRITICAL	MU_CAP_10UF
138S0625	3	CAP, 10UF, 6.3V, 20%, 0603	C1230,C1231,C1300	CRITICAL	MU_CAP_10UF
138S0625	9	CAP, 10UF, 6.3V, 20%, 0603	C2100,C2101,C2212,C2219,C2221,C2232,C2260,C2261,C2262	CRITICAL	MU_CAP_10UF
138S0625	5	CAP, 10UF, 6.3V, 20%, 0603	C2701,C2700,C2708,C2720,C2901	CRITICAL	MU_CAP_10UF
138S0625	6	CAP, 10UF, 6.3V, 20%, 0603	C5200,C5201,C5202,C5500,C5501,C5502	CRITICAL	MU_CAP_10UF
138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	C4100,C4400,C4613,C5000,C7201,C7301,C7350,C7351	CRITICAL	MU_CAP_10UF
138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	C7502,C7507,C7600,C7641,C7803,C7804,C7900,C7909	CRITICAL	MU_CAP_10UF
138S0625	5	CAP, 10UF, 6.3V, 20%, 0603	C8012,C8201,C8205,C8213,C8218	CRITICAL	MU_CAP_10UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0627	10	CAP, 10UF, 6.3V, 20%, 0603	C1300,C1301,C1302,C1303,C1304,C1305,C1306,C1307,C1308,C1309	CRITICAL	TY_CAP_10UF
138S0627	10	CAP, 10UF, 6.3V, 20%, 0603	C1210,C1211,C1212,C1213,C1214,C1215,C1216,C1217,C1218,C1219	CRITICAL	TY_CAP_10UF
138S0627	10	CAP, 10UF, 6.3V, 20%, 0603	C1220,C1221,C1222,C1223,C1224,C1225,C1226,C1227,C1228,C1229	CRITICAL	TY_CAP_10UF
138S0627	3	CAP, 10UF, 6.3V, 20%, 0603	C1230,C1231,C1300	CRITICAL	TY_CAP_10UF
138S0627	9	CAP, 10UF, 6.3V, 20%, 0603	C2100,C2101,C2212,C2219,C2221,C2232,C2260,C2261,C2262	CRITICAL	TY_CAP_10UF
138S0627	5	CAP, 10UF, 6.3V, 20%, 0603	C2701,C2700,C2708,C2720,C2901	CRITICAL	TY_CAP_10UF
138S0627	6	CAP, 10UF, 6.3V, 20%, 0603	C5200,C5201,C5202,C5500,C5501,C5502	CRITICAL	TY_CAP_10UF
138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	C4100,C4400,C4613,C5000,C7201,C7301,C7350,C7351	CRITICAL	TY_CAP_10UF
138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	C7502,C7507,C7600,C7641,C7803,C7804,C7900,C7909	CRITICAL	TY_CAP_10UF
138S0627	5	CAP, 10UF, 6.3V, 20%, 0603	C8012,C8201,C8205,C8213,C8218	CRITICAL	TY_CAP_10UF

Acoustic Cap BOM Config Tables

SYNC_MASTER=N/A SYNC_DATE=N/A

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SCALE	SHT	OF
NONE	5	109

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ICT Test Points

These nets have a ICT_TEST property This indicates a MUSTHAVE requirement for ICT

ICT_TEST

TRUE	PP18V5_DCIN	6 7 50 72	TRUE	BATT_POS	6 7 50	TRUE	PP3V3_S5	7 8 72	TRUE	PP3V42_G3H	6 7 8 72	TRUE	GND		TRUE	PM_SLP_S3_L	6 7 25 36 37 41 42 51 55
TRUE	PM_S4_STATE_L	6 25 35 41 58	TRUE	PM_SLP_S5_L	6 25 41 42	TRUE	SMC_PM_G2_EN	6 41 58	TRUE	IMVP_VR_ON	6 41 52	TRUE	GFX_VR_EN	6 9 53	TRUE	SMC_BATT_CHG_EN	6 41 42
TRUE	SMC_ONOFF_L	6 7 40 41 42	TRUE	ALL_SYS_PWRGD_AND	6 51	TRUE	PPVBAT_G3H_CHGR_REG	6 59 72	TRUE	CPU_PWRGD	6 10 13 23 66	TRUE	PM_RSMRST_L	6 25 41	TRUE	PM_PWRBTN_L	6 25 41
TRUE	TP_PCI_RST_L	9	TRUE	PLT_RST_L	6 7 24 28	TRUE	SMC_RESET_L	6 41 42 43	TRUE	PM_SYSRST_L	6 25 28 41	TRUE	PP1V5_S0	6 7 8 72	TRUE	PP1V8_S0	6 7 8 72
TRUE	PP1V05_S0	6 7 8 72	TRUE	PP1V8_S0	6 7 8 72	TRUE	PP1V8_S3	6 7 8 72	TRUE	PP0V9_S0	6 7 8 72	TRUE	PP0V9_S3	6 8 72	TRUE	PP1V25_S0	6 7 8 72
TRUE	PP5V_S5	6 7 8 72	TRUE	PP5V_S3	6 7 8 72	TRUE	PP5V_S0	6 7 8 72	TRUE	PP3V3_S3	6 7 8 72	TRUE	PP3V3_S0	6 7 8 72	TRUE	XDP_TCK	6 7 10 13 66
TRUE	XDP_TDI	6 7 10 13 66	TRUE	XDP_TDO	6 7 10 13 66	TRUE	XDP_TMS	6 7 10 13 66	TRUE	XDP_TRST_L	6 7 10 13 66	TRUE	XDP_CPURST_L	6 7 13 66	TRUE	XDP_BPM_L<4>	6 7 10 13 66
TRUE	XDP_BPM_L<5>	6 7 10 13 66	TRUE	XDP_DBRESET_L	6 7 10 13 28	TRUE	XDP_PWRGD	6 7 13	TRUE	SPI_A_SCLK_R	6 43 49 69	TRUE	SMC_MANUAL_RST_L	6 42	TRUE	SMC_TCK	6 41 42 43
TRUE	SMC_TDI	6 41 42 43	TRUE	SMC_TDO	6 41 42 43	TRUE	SMC_TMS	6 41 42 43	TRUE	SMC_RST_L	6 41 43	TRUE	CPU_A20M_L	6 10 23 66	TRUE	CPU_DPRSTP_L	6 10 16 23 52 66
TRUE	CPU_DPSLP_L	6 10 23 66	TRUE	CPU_FERR_L	6 10 23 66	TRUE	NB_BSEL<0>	6 7 13 16 30 66	TRUE	NB_BSEL<1>	6 7 13 16 30 66	TRUE	NB_BSEL<2>	6 7 13 16 30 66	TRUE	NB_CFG<16>	6 16
TRUE	NB_CFG<19>	6 16	TRUE	NB_CFG<20>	6 16												
TRUE	NB_CFG<3>	6 7 13 16	TRUE	NB_CFG<4>	6 7 13 16	TRUE	NB_CFG<5>	6 7 13 16	TRUE	NB_CFG<6>	6 7 13 16	TRUE	NB_CFG<7>	6 7 13 16	TRUE	NB_CFG<8>	6 7 13 16
TRUE	NB_CFG<9>	6 16	TRUE	NB_RESET_L	6 16 28	TRUE	NB_SB_SYNC_L	6 16 25	TRUE	NB_TEST1	6 16	TRUE	NB_TEST2	6 16	TRUE	1V05S0_RUNSS	51 54
TRUE	1V05S0_TRIP	54	TRUE	1V25S0_RUNSS	51 57	TRUE	1V51V05S0_V5FILT	54	TRUE	1V5S0_RUNSS	51 54	TRUE	1V5S0_TRIP	54	TRUE	1V8S3_CS	55
TRUE	1V8S3_V5FILT	55	TRUE	1V8S3_VDDQSET	55	TRUE	3V3S5_CS	56	TRUE	5V3V3S5_TONSEL	56	TRUE	5V3V3S5_V5FILT	56	TRUE	5V3V3S5_VREF	56
TRUE	5V3V3S5_VREG3	56	TRUE	5V5S_CS	56	TRUE	5V5S_VREG	56	TRUE	ADAPTER_SENSE	50	TRUE	AIRPORT_RST_L	7 28 36	TRUE	ALL_SYSPWRGD_DLY	51
TRUE	ALL_SYS_PWRGD	28 41 51 52	TRUE	ALL_SYS_PWRGD_AND	6 51	TRUE	ARB_DETECT_L	25	TRUE	AUD_MIC_CLK	7 37 60	TRUE	AUD_MIC_CLK_F	60	TRUE	AUD_MIC_DATA	7 37 60
TRUE	AUD_MIC_DATA_F	60	TRUE	BATT_POS	6 7 50	TRUE	BATT_POS_F	50 59	TRUE	BOOTROM_OVR_EN_L	23 25 43	TRUE	CHGR_AGATE	59	TRUE	CHGR_AMON	59
TRUE	CHGR_BGATE	59	TRUE	CHGR_BMON	59	TRUE	CHGR_BOOT	59	TRUE	CHGR_CSIN	59	TRUE	CHGR_CSIP	59	TRUE	CHGR_CSON	59
TRUE	CHGR_CSOP	59	TRUE	CHGR_DCIN	59	TRUE	CHGR_LOWCURRENT_GATE	59	TRUE	CHGR_LOWCURRENT_REF	59	TRUE	CHGR_SGATE	59	TRUE	CHGR_SGATE_DIV	59
TRUE	CHGR_VCOMP_R	59	TRUE	CHGR_VDD	59	TRUE	CHGR_VDDP	59	TRUE	CHGR_VNEG	59	TRUE	CHGR_VNEG_R	59	TRUE	CK505_CLK14P3M_TIMER	30 39
TRUE	CK505_FSA	30 71	TRUE	CK505_FSB_TEST_MODE	29 39	TRUE	CK505_FSC	30 71	TRUE	CK505_PCI3_CLK	29 30 71	TRUE	CK505_PCI5_FCTSEL1	29 30	TRUE	CK505_PCIF0_CLK	29 30
TRUE	CK505_PCIF1_CLK	29 30 71	TRUE	CK505_SRC_CLKREQ6_L	7 29 36	TRUE	CK505_USB48_FSA	29 30	TRUE	CK505_XTAL_OUT	29	TRUE	CLINK_NB_CLK	16 25 70	TRUE	CLINK_NB_DATA	16 25 70
TRUE	CLINK_NB_RESET_L	16 25 70	TRUE	CLK_PWRGD	25 29	TRUE	CPU_A20M_L	6 10 23 66	TRUE	CPU_BSEL<0>	10 30 66	TRUE	CPU_BSEL<1>	10 30 66	TRUE	CPU_BSEL<2>	10 30 66
TRUE	CPU_COMP<0>	10 66	TRUE	CPU_COMP<1>	10 66	TRUE	CPU_COMP<2>	10 66	TRUE	CPU_COMP<3>	10 66	TRUE	CPU_DPRSTP_L	6 10 16 23 52 66	TRUE	CPU_DPSLP_L	6 10 23 66
TRUE	CPU_FERR_L	6 10 23 66	TRUE	CPU_GTLREF	10 66	TRUE	CPU_IERR_L	10 66	TRUE	CPU_IGNNE_L	10 23 66	TRUE	CPU_INIT_L	10 23 66	TRUE	CPU_INTR	10 23 66
TRUE	CPU_NMI	10 23 66	TRUE	CPU_PROCHOT_BUF	42	TRUE	CPU_PROCHOT_L	10 42 52 66	TRUE	CPU_PROCHOT_L_R	42	TRUE	CPU_PWRGD	6 10 13 23 66	TRUE	CPU_SMI_L	10 23 66
TRUE	CPU_STPCLK_L	10 23 66	TRUE	CPU_THERMD_N	10 46 66	TRUE	CPU_THERMD_P	10 46 66	TRUE	CPU_THERMTRIP_R	23	TRUE	CPU_VCCSENSE_N	11 52 66	TRUE	CPU_VCCSENSE_P	11 52 66
TRUE	CPU_VID<6..0>	11 12 52 66	TRUE	CRT_BLUE	63 67	TRUE	CRT_GREEN	63 67	TRUE	CRT_HSYNC_LS	63	TRUE	CRT_HSYNC_LS_R	63	TRUE	CRT_HSYNC_R	63 67
TRUE	CRT_RED	63 67	TRUE	CRT_TVO_IREF	63 67	TRUE	CRT_VSYNC_LS	63	TRUE	CRT_VSYNC_LS_R	63	TRUE	CRT_VSYNC_R	63 67	TRUE	DEBUG_RESET_L	28 43
TRUE	DLY_OFF_A	51	TRUE	DLY_OFF_B	51	TRUE	DLY_OFF_C	51	TRUE	DLY_OFF_D	51	TRUE	DMI_IRCOMP_R	24	TRUE	DMI_N2S_N<3..0>	16 24 67
TRUE	DMI_N2S_P<3..0>	16 24 67	TRUE	DMI_S2N_N<3..0>	16 24 67	TRUE	DMI_S2N_P<3..0>	16 24 67	TRUE	DVI_HOST	7 37 63	TRUE	DVI_HOTPLUG_DET	24 61 62	TRUE	DVI_HOTPLUG_DET_BUF	61 62
TRUE	DVI_HOTPLUG_DET_DEL_L	62	TRUE	DVI_HOTPLUG_DET_INT_L	62	TRUE	DVI_HPDET_RC	62	TRUE	EXCARD_OC_L	24	TRUE	EXTAUSB_OC_F_L	39	TRUE	EXTAUSB_OC_L	9
TRUE	EXTBUSB_OC_L	9	TRUE	EXTGPU_LVDS_EN	7 13 24	TRUE	EXT_COMPVID_B	63 67	TRUE	EXT_C_R	63 67	TRUE	EXT_Y_G	63 67	TRUE	FAN_RT_PWM	7 47
TRUE	FAN_RT_TACH	7 47	TRUE	FRANKCARD_GPIO	25 43	TRUE	FSB_CLK_CPU_N	10 30 71	TRUE	FSB_CLK_CPU_P	10 30 71	TRUE	FSB_CLK_NB_N	14 30 71	TRUE	FSB_CLK_NB_P	14 30 71
TRUE	FSB_CPURST_L	10 13 14 66	TRUE	FWH_MFG_MODE	25	TRUE	GCORE_BST_D	53	TRUE	GCORE_COMP_R	53	TRUE	GCORE_CSFB	53	TRUE	GCORE_FBRTN	53
TRUE	GCORE_LLINE	53	TRUE	GCORE_PMON	53	TRUE	GCORE_PMONFS	53	TRUE	GCORE_PWRGD	53	TRUE	GCORE_RAMP	53	TRUE	GCORE_RPM	53
TRUE	GCORE_RT	53	TRUE	GCORE_ST	53	TRUE	GCORE_SW	53	TRUE	GCORE_SW_R	53	TRUE	GCORE_VARFREQ	53	TRUE	GCORE_VCC	53
TRUE	GCORE_VDC_DIV	53	TRUE	GCORE_VRPM	53	TRUE	GFX_VID<3..0>	16 22 53	TRUE	GFX_VR_EN	6 9 53	TRUE	GLAN_COMP	23 70	TRUE	GND_1V51V05S0_SGND	54
TRUE	GND_1V8S3_CSGND	55	TRUE	GND_1V8S3_SGND	55	TRUE	GND_5V3V3S5_SGND	56	TRUE	GND_ALS_F	51	TRUE	GND_CHGR_SGND	59	TRUE	GND_GCORE_PGND	53
TRUE	GND_IMVP6_SGND	52	TRUE	GND_LCDBKLT_GNDA	64	TRUE	GND_P1V2S3_SGND	57	TRUE	GND_SMC_AVSS	41 42 45 53 59	TRUE	HDA_BIT_CLK	9 23 69	TRUE	HDA_BIT_CLK_R	23 69
TRUE	HDA_DOCK_EN_L	23	TRUE	HDA_RST_L	9 23 37 69	TRUE	HDA_RST_L_R	23 69	TRUE	HDA_SDIN0	9 23 69	TRUE	HDA_SDIN1		TRUE	HDA_SDOUT	9 23 69
TRUE	HDA_SDOUT_R	23 69	TRUE	HDA_SYNC	7 9 23 37 69	TRUE	HDA_SYNC_R	23 69	TRUE	HDMI_HOST	7 37 63	TRUE	I2C_TOP_ALS_SDA	60	TRUE	I2C_TOP_ALS_SDA_F	60
TRUE	IDE_IRQ14	23 38 69	TRUE	IDE_PDA<2..0>	23 38 69	TRUE	IDE_PDCS1_L	23 38 69	TRUE	IDE_PDCS3_L	23 38 69	TRUE	IDE_PDD<15..0>	23 38 69	TRUE	IDE_PDDACK_L	23 38 69
TRUE	IDE_PDDREQ	23 38 69	TRUE	IDE_PDIORDY	23 38 69	TRUE	IDE_PDIOR_L	23 38 69	TRUE	IDE_PDIOW_L	23 38 69	TRUE	IDE_RESET_BUF_L	38	TRUE	IDE_RESET_L	24 38
TRUE	IMVP6_BOOT	52	TRUE	IMVP6_BOOT_RC	52	TRUE	IMVP6_COMP_R	52	TRUE	IMVP6_DROOP	52	TRUE	IMVP6_PHASE	52	TRUE	IMVP6_PVCC	52
TRUE	IMVP6_RBIAS	52	TRUE	IMVP6_SOFT	52	TRUE	IMVP6_VDIFF	52	TRUE	IMVP6_VDIFF_RC	52	TRUE	IMVP6_VO_R	52	TRUE	IMVP6_VR_TT	52
TRUE	IMVP6_VSEN_N	52 66	TRUE	IMVP6_VSEN_P	52 66	TRUE	IMVP6_VSUM	52	TRUE	IMVP6_VW	52	TRUE	IMVP_DPRSLPVR	52 66	TRUE	IMVP_VR_ON	6 41 52
TRUE	INT_PIRQA_L	24 70	TRUE	INT_PIRQB_L	24 70	TRUE	INT_PIRQC_L	24 70	TRUE	INT_PIRQD_L	24 70	TRUE	INT_PIRQE_L	24 70	TRUE	INT_PIRQF_L	24 70
TRUE	INT_SERIRQ	25 41 43	TRUE	LAN_ENERGY_DET	23	TRUE	LAN_PHYPC	23 25	TRUE	LCDBKLT_ENA	64	TRUE	LCDBKLT_ISET	64	TRUE	LCDBKLT_OVP	64
TRUE	LCDBKLT_PWM_UNBUF	9 64	TRUE	LCDBKLT_PWREN	9 64	TRUE	LCDBKLT_RT	64	TRUE	LCDBKLT_RTN<6..1>	7 60 64	TRUE	LCDBKLT_RTN_RC<6..1>	64	TRUE	LCDBKLT_SSTCMP	64
TRUE	LCDBKLT_SSTCMP_RC	64	TRUE	LCDBKLT_VREF	64	TRUE	LCDVDD_PWREN_L	60	TRUE	LCDVDD_PWREN_L_R	60	TRUE	LOCAL_CTRL_CLK	7 13 15	TRUE	LOCAL_CTRL_DATA	7 13 15
TRUE	LPC_AD<3..0>	23 41 43	TRUE	LPC_FRAME_L	23 41 43	TRUE	LSOC_H		TRUE	LSOC_H_R	7	TRUE	LVDS_A_CLK_F_N	7 60	TRUE	LVDS_A_CLK_F_P	7 60
TRUE	LVDS_A_CLK_N	15 60 67	TRUE	LVDS_A_CLK_P	15 60 67	TRUE	LVDS_A_DATA_F_N<2..0>	60 67	TRUE	LVDS_A_DATA_F_P<2..0>	60 67	TRUE	LVDS_A_DATA_N<2>	7 15 60 67	TRUE	LVDS_A_DATA_P<2>	7 15 60 67
TRUE	LVDS_DDC_CLK	7 15 60	TRUE	LVDS_DDC_DATA	7 15 60	TRUE	LVDS_IBG	15 60 67	TRUE	LVDS_VDD_EN	15 60	TRUE	MEM_ODT<3..0>	16 31 32 33 68	TRUE	MEM_RCOMP	16
TRUE	MEM_RCOMP_L	16	TRUE	MEM_RCOMP_VOH	16	TRUE	MEM_RCOMP_VOL	16	TRUE	NB_BSEL<0>	6 7 13 16 30 66	TRUE	NB_BSEL<1>	6 7 13 16 30 66	TRUE	NB_BSEL<2>	6 7 13 16 30 66
TRUE	NB_CFG<16>	6 16	TRUE	NB_CFG<19>	6 16	TRUE	NB_CFG<20>	6 16	TRUE	NB_CFG<3>	6 7 13 16	TRUE	NB_CFG<4>	6 7 13 16	TRUE	NB_CFG<5>	6 7 13 16
TRUE	NB_CFG<6>	6 7 13 16	TRUE	NB_CFG<7>	6 7 13 16	TRUE	NB_CFG<8>	6 7 13 16	TRUE	NB_CFG<9>	6 16	TRUE	NB_CLINK_VREF	16 70	TRUE	NB_CLK100M_DPLLSS_N	9 30 71
TRUE	NB_CLK100M_DPLLSS_P	9 30 71	TRUE	NB_CLK100M_PCIE_N	16 30 71	TRUE	NB_CLK100M_PCIE_P	16 30 71	TRUE	NB_CLK96M_DOT_N	9 30 71	TRUE	NB_CLK96M_DOT_P	9 30 71	TRUE	NB_CLKREQ_L	16 29
TRUE	NB_FSB_RCOMP	14	TRUE	NB_FSB_SCOMP	14	TRUE	NB_FSB_SCOMP_L	14	TRUE	NB_FSB_SWING	14	TRUE	NB_FSB_VREF	14	TRUE	NB_RESET_L	6 16 28
TRUE	NB_SB_SYNC_L	6 16 25	TRUE	NB_TEST1	6 16	TRUE	NB_TEST2	6 16	TRUE	NB_VCCSM_LF1	18 68	TRUE	NB_VCCSM_LF2	18 68	TRUE	NB_VCCSM_LF3	18 68
TRUE	NB_VCCSM_LF4	18 68	TRUE	NB_VCCSM_LF5	18 68	TRUE	NB_VCCSM_LF6	18 68	TRUE	NB_VCCSM_LF7	18 68	TRUE	NB_VTTLF_CAP1	19	TRUE	NB_VTTLF_CAP2	19
TRUE	NB_VTTLF_CAP3	19	TRUE	ODD_PWR_EN_L	24	TRUE	ONEWIRE_DCIN_DIV	50	TRUE	ONEWIRE_EN	50	TRUE	ONEWIRE_ESD	50	TRUE	ONEWIRE_OV	50
TRUE	ONEWIRE_PWR_EN_L	50	TRUE	ONEWIRE_PWR_EN_L_DIV	50	TRUE	P1V2S5S0NBDPLL_FB	22	TRUE	P1V2S5S0NBDPLL_RF	22	TRUE	P1V2S5S0_ITH	57	TRUE	P1V2S5S0_ITH_RC	57
TRUE	P1V2S5S0_MODE	57	TRUE	P1V2S5S0_RT	57	TRUE	P1V8S0_EN	51	TRUE	P3V3S0_EN	51	TRUE	P3V3S3_EN_L	58	TRUE	P3V3TVDAC_EN_RC	22
TRUE	P3V3TVDAC_NOISE	22	TRUE	P3V42G3H5_BOOST	57	TRUE	P3V42G3H_SHDN_L	57	TRUE	P3V42G3H_SHDN_L1	57	TRUE	P5VS0_EN	51	TRUE	P5VS3_EN_L	58
TRUE	PBUS_ISENSE_IN_NEG	59	TRUE	PBUS_ISENSE_VREG	59	TRUE	PBUS_S0_SMC_VSENSE	45	TRUE	PBUS_SMC_VSENSE_EN_L	16	TRUE	PCIE_CLK100M_MINI_N	72 73	TRUE	PCIE_CLK100M_MINI_N_F	7 36
TRUE	PCIE_CLK100M_MINI_P	72 73	TRUE	PCIE_CLK100M_MINI_P_F	7 36	TRUE	PCIE_E_D2R_N	36	TRUE	PCIE_E_D2R_N_F	7 36	TRUE	PCIE_E_D2R_P	36	TRUE	PCIE_E_D2R_P_F	7 36
TRUE	PCIE_E_R2D_C_N	36	TRUE	PCIE_E_R2D_C_N_F	7 36	TRUE	PCIE_E_R2D_C_P	36	TRUE	PCIE_E_R2D_C_P_F	7 36	TRUE	PCIE_E_R2D_N	36	TRUE	PCIE_E_R2D_P	36
TRUE	PCIE_WAKE_L	7 25 36	TRUE	PCI_CLK33M_LPCPLUS	30 43 73	TRUE	PCI_CLK33M_SB	24 30 71	TRUE	PCI_CLK33M_SMC	30 41 71	TRUE	PCI_DEVSEL_L	24 70	TRUE	PCI_FRAME_L	24 70
TRUE	PCI_FW_GNT_L	24 70	TRUE	PCI_FW_REQ_L	24 70	TRUE	PCI_IRDY_L	24 70	TRUE	PCI_LOCK_L	24 70	TRUE	PCI_PERR_L	24 70	TRUE	PCI_PME_FW_L	25
TRUE	PCI_REQ0_L	24 70	TRUE	PCI_REQ2_L	24 70	TRUE	PCI_SERR_L	24 70	TRUE	PCI_STOP_L	24 70	TRUE	PCI_TRDY_L	24 70	TRUE	PEG_COMP	15
TRUE	PEG_D2R_N<1>	15 61 67	TRUE	PEG_D2R_P<1>	15 61 67	TRUE	PEG_R2D_C_N<3..0>	15 61 67	TRUE	PEG_R2D_C_P<3..0>	15 61 67	TRUE	PGOOD_1V25S0	51	TRUE	PGOOD_1V8S3	51 55
TRUE	PLT_RST_BUF_L	28	TRUE	PLT_RST_L	6 7 24 28	TRUE	PM_BATLOW_L	25 41	TRUE	PM_BMBUSY_L	22 72	TRUE	PM_CLKRUN_L	25 41 43	TRUE	PM_DPRSLPVR	16 25 52 66
TRUE	PM_EXTTS_L<0>	16 41	TRUE	PM_EXTTS_L<1>	16 41	TRUE	PM_LAN_ENABLE	25 41	TRUE	PM_LAN_PWRGD	41 42	TRUE	PM_LATRIGGER_L	7 13 24	TRUE	PM_PWRBTN_L	6 25 41
TRUE	PM_RI_L	25	TRUE	PM_RSMRST_L	6 25 41	TRUE	PM_S4_STATE_L	6 25 35 41 58	TRUE	PM_SB_PWROK	9 25 28	TRUE	PM_SLP_S3_L	6 7 25 36 41 51 55 57	TRUE	PM_SLP_S4_L	52 57
TRUE	PM_SLP_S5_L	6 25 41 42	TRUE	PM_STPCPU_L	25 29 30	TRUE	PM_STPPCI_L	25 29 30	TRUE	PM_SUS_STAT_L	25 41 43	TRUE	PM_SYSRST_L	6 25 28 43	TRUE	PM_THRMTRIP_L	10 16 23 42 66
TRUE	PM_THRM_L	25	TRUE	PM_WLAN_EN_L	36	TRUE	PM_WLAN_EN_L1	36	TRUE	PM_WLAN_EN_L2	36	TRUE	PM_WLAN_EN_L_SS	36	TRUE	PP0V9_S0	6 7 8 72
TRUE	PP0V9_S3	6 8 72	TRUE	PP18V5_DCIN	6 7 50 72	TRUE	PP18V5_DCIN_ONEWIRE	50 72	TRUE	PP18V5_G3H	7 8 72	TRUE	PP18V5_S5_CHGR_SW_R	59 72	TRUE	PP1V05_S0	6 7 8 72
TRUE	PP1V05_S0_NB_VCCPEG	15 19 21 72	TRUE	PP1V25_S0	6 7 8 72	TRUE	PP1V25_S0M_NB_VCCA_HPLL	19 21 72	TRUE	PP1V25_S0_NB_DPLL	22 72	TRUE	PP1V25_S0_NB_PEGPLL	19 21 72	TRUE	PP1V25_S0_NB_PEGPLL_RC	21 72
TRUE	PP1V25_S0_NB_VCCA_DPLLA	19 22 72	TRUE	PP1V25_S0_NB_VCCA_DPLLB	19 22 72	TRUE	PP1V5_S0	6 7 8 72	TRUE	PP1V5_S0_NB_QDAC	22 72	TRUE	PP1V5_S0_NB_VCCD_CRT	22 72	TRUE	PP1V5_S0_NB_VCCD_QDAC	19 22 72
TRUE	PP1V5_S0_SB_VCC1_5_B	23 24 26 27 72	TRUE	PP1V5_S0_SB_VCCD1PLL	26 27 72	TRUE	PP1V5_S0_SB_VCCD1PLL_F	27 72	TRUE	PP1V5_S0_SB_VCCD2PLL	26 27 72	TRUE	PP1V5_S0_SB_VCCSATAPLL	26 27 72	TRUE	PP1V8_S0	6 7 8 72
TRUE	PP1V8_S0_ANALOG_SDVO_F	61 72	TRUE	PP1V8_S0_ANALOG_TMDS_F	61 72	TRUE	PP1V8_S0_NB_VCCTXLVDS	19 22 72	TRUE	PP1V8_S0_PVCC1_TMDS_F	61 72	TRUE	PP1V8_S0_PVCC2_TMDS_F	61 72	TRUE	PP1V8_S0_TMDS_F	61 72
TRUE	PP1V8_S3	6 7 8 72	TRUE	PP1V8_S3M_NB_VCCSMCK	19 21 72	TRUE	PP1V8_S3_NB_VCCSMCK_RC	21 72	TRUE	PP3V3_A_S0	6 8	TRUE	PP3V3_B_S0	6 8	TRUE	PP3V3_LCDVDD_SW	60 72
TRUE	PP3V3_LCDVDD_SW_F	7 60 72	TRUE	PP3V3_S0_ANALOG_SDVO_F	61 72	TRUE	PP3V3_S0_CK505_VDD48	72	TRUE	PP3V3_S0_CK505_VDDA	72	TRUE	PP3V3_S0_CK505_VDDA_R	72	TRUE	PP3V3_S0_CK505_VDD_CPU_SRC	29 72
TRUE	PP3V3_S0_CK505_VDD_PCI	72	TRUE	PP3V3_S0_CK505_VDD_REF	72	TRUE	PP3V3_S0_HDCP_F	62	TRUE	PP3V3_S0_IMVP6_3V3	52 72	TRUE	PP3V3_S0_LCD_F	7 60 72	TRUE	PP3V3_S0_NBCORE_FOLLOW_R	21 72
TRUE	PP3V3_S0_NB_CRTDAC_F	22 72	TRUE	PP3V3_S0_NB_TVDAC	22 72	TRUE	PP3V3_S0_NB_TVDAC_F	22 72	TRUE	PP3V3_S0_NB_TVDAC_FOLLOW	22 72	TRUE	PP3V3_S0_NB_VCCA_CRTDAC	19 22 72	TRUE	PP3V3_S0_NB_VCCA_DAC_BG	19 22 72
TRUE	PP3V3_S0_NB_VCCA_TVDACA	19 22 72	TRUE	PP3V3_S0_NB_VCCA_TVDACB	19 22 72	TRUE	PP3V3_S0_NB_VCCA_TVDACC	19 22 72	TRUE	PP3V3_S0_SPVCC_TMDS_F	61 72	TRUE	PP3V3_S3	6 7 8 72	TRUE	PP3V3_S3_ALS_F	
TRUE	PP3V3_S3_AP_AUX	7 36 72	TRUE	PP3V3_S5_AVREF_SMC	41 42 72	TRUE	PP3V3_S5_SMC_AVCC	41 72	TRUE	PP3V42G3H_SW	57 72	TRUE	PP3V42_G3H	6 7 8 72	TRUE	PP3V42_G3H_IPD_F	7 40
TRUE	PP3V42_G3H_SMCUSBMUX_R	39 72	TRUE	PP5V_S0	6 7 8 72	TRUE	PP5V_S0_DVIPORT	7 37 63 72	TRUE	PP5V_S0_DVIPORT_D	63 72	TRUE	PP5V_S0_IMVP6_VDD	52 72	TRUE	PP5V_S0_KBDLED_F	7 40 72
TRUE	PP5V_S0_SB_V5REF	26 27 72	TRUE	PP5V_S0_TMDS_FUSE	63 72	TRUE	PP5V_S3	6 7 8 72	TRUE	PP5V_S3_CAMERA_F	7 60 72	TRUE	PP5V_S3_TOPCASE_F	7 40	TRUE	PP5V_S3_USB2_EXTA	39 72
TRUE	PP5V_S3_USB2_EXTA_F	7 37 39 72	TRUE	PP5V_S5	6 7 8 72	TRUE	PP5V_S5_SB_V5REF_SUS	26 27 72	TRUE	PPBUS_G3H	7 8 72	TRUE	PPBUS_R_G3H	7 8 72	TRUE	PPDCIN_G3H	7 8 72
TRUE	PPDCIN_G3H_R	50 72	TRUE	PPVBATT_G3H_R	50 72	TRUE	PPVBAT_G3H_CHGR_OUT	59 72	TRUE	PPVBAT_G3H_CHGR_REG	6 59 72	TRUE	PPVBAT_G3H_CHRGR_REG_0	59 72	TRUE	PPVBAT_G3H_CHRGR_REG_R	59 72
TRUE	PPVCORE_S0_CPU	6 7 8 72	TRUE	PPVCORE_S0_NB_GFX	6 7 8 72	TRUE	PPVDCIN_G3H_PRE	45 59 72	TRUE	PPVDCIN_G3H_PRE2	59 72	TRUE	PPVDCIN_G3H_PRE_0	59 72	TRUE	PPVDCIN_G3H_PRE_R	59 72
TRUE	PPVIN_S5_IMVP6_VIN	52 72	TRUE	PPVOUT_S0_LCDBKLT	7 60 64 72	TRUE	PPVOUT_S0_LCDBKLT_SW	64 72	TRUE	RSMRST_PWRGD	41 42 56	TRUE	RSVD_EXTGPU_LVDS_EN	25	TRUE	RUNSS_GATE_D	51
TRUE	RUNSS_GATE_D_L	51	TRUE	S0PWRGD_1V8_DIV	51	TRUE	S0PWRGD_3V3_DIV	51	TRUE	S0PWRGD_5V_DIV	51	TRUE	S0SEQ_BEGIN	51	TRUE	SATA_B_DET_L	25
TRUE	SB_A20GATE	23	TRUE	SB_CLINK_VREF0	25 70	TRUE	SB_CLINK_VREF1	25 70	TRUE	SB_CLK100M_DMI_N	24 30 71	TRUE	SB_CLK100M_DMI_P	24 30 71	TRUE	SB_CLK14P3M_TIMER	25 30 71
TRUE	SB_CLK48M_USBCTLR	25 30 71	TRUE	SB_CRT_TVOUT_MUX_L	25 63	TRUE	SB_GPIO10_CL1	23 25	TRUE	SB_GPIO18	25	TRUE	SB_GPIO30	7 13 24	TRUE	SB_GPIO36	25
TRUE	SB_GPIO40	7 13 24	TRUE	SB_INTVRMEN	23	TRUE	SB_LAN100_SLP	23	TRUE	SB_RCIN_L	23	TRUE	SB_RTC_RST_L	23 28	TRUE	SB_RTC_X1	23 28
TRUE	SB_RTC_X1_R	28	TRUE	SB_RTC_X2	23 28	TRUE	SB_SLOAD	25	TRUE	SB_SM_INTRUDER_L	23 28	TRUE	SB_SPKR	25	TRUE	SDVO_CTRLCLK	16 61
TRUE	SDVO_CTRLDATA	16 61	TRUE	SMBUS_SB_ME_SCL	44	TRUE	SMBUS_SB_ME_SDA	44	TRUE	SMBUS_SB_SCL	44	TRUE	SMBUS_SB_SDA	44	TRUE	SMBUS_SMC_0_S0_SCL	7 44 71
TRUE	SMBUS_SMC_0_S0_SDA	7 44 71	TRUE	SMBUS_SMC_A_S3_SCL	44 71	TRUE	SMBUS_SMC_A_S3_SDA	44 71	TRUE	SMBUS_SMC_BSA_SCL	7 44 71	TRUE	SMBUS_SMC_BSA_SDA	7 44 71	TRUE	SMBUS_SMC_B_S3_SCL	44
TRUE	SMBUS_SMC_B_S3_SDA	44	TRUE	SMBUS_SMC_MGMT_SCL	44 71	TRUE	SMBUS_SMC_MGMT_SDA	44 71	TRUE	SMB_AIRPORT_CONN_CLK	7 36	TRUE	SMB_AIRPORT_CONN_DATA	7 36	TRUE	SMC_ACIN_VSENSE	41 45
TRUE	SMC_ADAPTER_EN	9 41 42	TRUE	SMC_BATTPACK_STAT	41 42	TRUE	SMC_BATT_CHG_EN	6 41 42	TRUE	SMC_BATT_ISENSE	41 59	TRUE	SMC_BC_ACOK	42 50	TRUE	SMC_BC_ACOK_ONEWIRE_R	50
TRUE	SMC_BS_ALRT_L	7 41 42 56	TRUE	SMC_CASE_OPEN	41 42	TRUE	SMC_DCIN_ISENSE	41 59	TRUE	SMC_EXTAL	41 42	TRUE	SMC_FAN_0_CTL	41 47	TRUE	SMC_FAN_0_TACH	41 47
TRUE	SMC_GPU_ISENSE	41 53	TRUE	SMC_GPU_VSENSE	41 45	TRUE	SMC_KBC_MDE	41	TRUE	SMC_LID	7 40 41 42	TRUE	S

Functional Test Points

NB NO_TESTS

These are normally testpoints but become NC

NO_TEST

T210	TRUE	TP_LVDS_VBG	NC_LVDS_VBG	MAKE_BASE=TRUE
T1245	TRUE	TP_NB_RSVD<31>	NC_NB_RSVD_31	MAKE_BASE=TRUE
T1255	TRUE	TP_NB_RSVD<32>	NC_NB_RSVD_32	MAKE_BASE=TRUE
T1257	TRUE	TP_NB_RSVD<33>	NC_NB_RSVD_33	MAKE_BASE=TRUE
T1270	TRUE	TP_MEM_A_RCVEN_L	NC_MEM_A_RCVEN_L	MAKE_BASE=TRUE
T1280	TRUE	TP_MEM_B_RCVEN_L	NC_MEM_B_RCVEN_L	MAKE_BASE=TRUE
T237	TRUE	TP_NB_RSVD<1>	NC_NB_RSVD_1	MAKE_BASE=TRUE
T238	TRUE	TP_NB_RSVD<2>	NC_NB_RSVD_2	MAKE_BASE=TRUE
T1272	TRUE	TP_NB_RSVD<3>	NC_NB_RSVD_3	MAKE_BASE=TRUE
T1274	TRUE	TP_NB_RSVD<4>	NC_NB_RSVD_4	MAKE_BASE=TRUE
T1277	TRUE	TP_NB_RSVD<5>	NC_NB_RSVD_5	MAKE_BASE=TRUE
T1279	TRUE	TP_NB_RSVD<6>	NC_NB_RSVD_6	MAKE_BASE=TRUE
T1282	TRUE	TP_NB_RSVD<7>	NC_NB_RSVD_7	MAKE_BASE=TRUE
T1286	TRUE	TP_NB_RSVD<8>	NC_NB_RSVD_8	MAKE_BASE=TRUE
T1241	TRUE	TP_NB_RSVD<14>	NC_NB_RSVD_14	MAKE_BASE=TRUE
T1243	TRUE	TP_NB_RSVD<21>	NC_NB_RSVD_21	MAKE_BASE=TRUE
T1305	TRUE	TP_NB_RSVD<22>	NC_NB_RSVD_22	MAKE_BASE=TRUE
T1307	TRUE	TP_NB_RSVD<23>	NC_NB_RSVD_23	MAKE_BASE=TRUE
T1309	TRUE	TP_NB_RSVD<24>	NC_NB_RSVD_24	MAKE_BASE=TRUE
T1312	TRUE	TP_NB_RSVD<25>	NC_NB_RSVD_25	MAKE_BASE=TRUE
T1314	TRUE	TP_NB_RSVD<26>	NC_NB_RSVD_26	MAKE_BASE=TRUE
T1316	TRUE	TP_NB_RSVD<27>	NC_NB_RSVD_27	MAKE_BASE=TRUE
T1285	TRUE	TP_NB_RSVD<35>	NC_NB_RSVD_35	MAKE_BASE=TRUE
T1287	TRUE	TP_NB_RSVD<36>	NC_NB_RSVD_36	MAKE_BASE=TRUE
T1288	TRUE	TP_NB_CFG<10>	NC_NB_CFG_10	MAKE_BASE=TRUE
T1290	TRUE	TP_NB_CFG<11>	NC_NB_CFG_11	MAKE_BASE=TRUE
T1291	TRUE	TP_NB_CFG<14>	NC_NB_CFG_14	MAKE_BASE=TRUE
T1293	TRUE	TP_NB_CFG<15>	NC_NB_CFG_15	MAKE_BASE=TRUE
T1295	TRUE	TP_NB_CFG<17>	NC_NB_CFG_17	MAKE_BASE=TRUE
T1297	TRUE	TP_NB_NC<1>	NC_NB_NC_1	MAKE_BASE=TRUE
T1320	TRUE	TP_NB_NC<2>	NC_NB_NC_2	MAKE_BASE=TRUE
T1321	TRUE	TP_NB_NC<3>	NC_NB_NC_3	MAKE_BASE=TRUE
T1323	TRUE	TP_NB_NC<4>	NC_NB_NC_4	MAKE_BASE=TRUE
T1325	TRUE	TP_NB_NC<5>	NC_NB_NC_5	MAKE_BASE=TRUE
T1327	TRUE	TP_NB_NC<6>	NC_NB_NC_6	MAKE_BASE=TRUE
T1329	TRUE	TP_NB_NC<7>	NC_NB_NC_7	MAKE_BASE=TRUE
T1340	TRUE	TP_NB_NC<8>	NC_NB_NC_8	MAKE_BASE=TRUE
T1342	TRUE	TP_NB_NC<9>	NC_NB_NC_9	MAKE_BASE=TRUE
T1344	TRUE	TP_NB_NC<10>	NC_NB_NC_10	MAKE_BASE=TRUE
T1332	TRUE	TP_NB_NC<11>	NC_NB_NC_11	MAKE_BASE=TRUE
T1334	TRUE	TP_NB_NC<12>	NC_NB_NC_12	MAKE_BASE=TRUE
T1336	TRUE	TP_NB_NC<13>	NC_NB_NC_13	MAKE_BASE=TRUE
T1346	TRUE	TP_NB_NC<14>	NC_NB_NC_14	MAKE_BASE=TRUE
T1348	TRUE	TP_NB_RSVD<29>	NC_NB_RSVD_29	MAKE_BASE=TRUE
T1350	TRUE	TP_NB_RSVD<28>	NC_NB_RSVD_28	MAKE_BASE=TRUE
T1352	TRUE	TP_NB_RSVD<30>	NC_NB_RSVD_30	MAKE_BASE=TRUE
T1308	TRUE	TP_NB_RSVD<30>	NC_NB_RSVD_30	MAKE_BASE=TRUE
T1431	TRUE	CRT_DDC_CLK	NC_CRT_DDC_CLK	MAKE_BASE=TRUE
T1432	TRUE	CRT_DDC_DATA	NC_CRT_DDC_DATA	MAKE_BASE=TRUE

Power Supply NO_TESTs

NO_TEST

CLOCK NO_TESTS

NO_TEST

LVDS NO_TESTS

NO_TEST

REQUIRED NETS

FUNC TEST - BATTERY CONNECTOR

x3	T1647	TRUE	BATT_POS	6 50
x3	T1649	TRUE	GND	
	T1638	TRUE	SMC_BS_ALRT_L	6 41 42 50
	T1646	TRUE	SMBUS_SMC_BSA_SCL	6 44 71
	T1639	TRUE	SMBUS_SMC_BSA_SDA	6 44 71

FUNC TEST - DC-IN CONNECTOR

x2	T1648	TRUE	PP18V5_DCIN	6 50 72
	T1655	TRUE	SYS_ONEWIRE	6 41 42 50
x2	T1706	TRUE	GND	

FUNC TEST - TEMP SENSOR CONNECTOR

	T1671	TRUE	SMBUS_SMC_0_S0_SCL	6 44 71
	T1672	TRUE	SMBUS_SMC_0_S0_SDA	6 44 71
	T1675	TRUE	=PP3V3_S0_THRM_SNR	8 46

FUNC TEST - FAN CONNECTOR

	T1666	TRUE	=PP5V_S0_FAN	8 47
	T1667	TRUE	FAN_RT_PWM	6 47
	T1669	TRUE	FAN_RT_TACH	6 47
	T1713	TRUE	GND	

FUNC TEST - CAMERA USB, LVDS, ALS

x2	T1654	TRUE	PP5V_S3_CAMERA_F	6 60 72
	T1653	TRUE	USB2_CAMERA_F_P	6 60 69
	T1656	TRUE	USB2_CAMERA_F_N	6 60 69
	T1657	TRUE	LCDBKLT_RTN<1..6>	6 60 64
	T1658	TRUE	LVDS_A_DATA_N<0..2>	6 15 60 67
	T1659	TRUE	LVDS_A_DATA_P<0..2>	6 15 60 67
	T1660	TRUE	PPVOUT_S0_LCDBKLT	6 60 64 72
	T1661	TRUE	LVDS_A_CLK_F_N	6 60
	T1662	TRUE	LVDS_A_CLK_F_P	6 60
	T1663	TRUE	LVDS_DDC_CLK	6 15 60
	T1664	TRUE	LVDS_DDC_DATA	6 15 60
	T1665	TRUE	PP3V3_S0_LCD_F	6 60 72
x2	T1666	TRUE	PP3V3_LCDVDD_SW_F	6 60 72
	T1711	TRUE	=I2C_TOP_ALS_SDA	44 60
	T1712	TRUE	=I2C_TOP_ALS_SCL	44 60
x10	T1715	TRUE	GND	

FUNC TEST - AUDIO CONNECTOR

	T1645	TRUE	HDA_SYNC	6 9 23 37 69
	T1648	TRUE	HDA_BITCLK	9 37
	T1735	TRUE	AUD_MIC_DATA	6 37 60
	T1730	TRUE	HDA_SDATAOUT	9 37
	T1737	TRUE	=PPVIN_S0_AUDIO	8 37
	T1731	TRUE	HDA_SDATAIN0	9 37
	T1740	TRUE	AUD_MIC_CLK	6 37 60
	T1739	TRUE	PM_SLP_S3_L	6 25 36 37 41 42 51 55

FUNC TEST - IPD CONNECTOR

	T1507	TRUE	SMC_LID	6 40 41 42
	T1508	TRUE	PP3V42_G3H_IPD_F	6 40
	T1509	TRUE	SMC_SYS_KBDLED	6 40 41
	T1507	TRUE	SMC_SYS_LED	6 40 41
	T1510	TRUE	=USB2_TRACKPAD_N	9 40
	T1512	TRUE	=USB2_TRACKPAD_P	9 40
	T1511	TRUE	SMC_ONOFF_L	6 7 40 41 42
	T1513	TRUE	=USB2_IR_N	7 9 40
	T1514	TRUE	=USB2_IR_P	7 9 40
	T1515	TRUE	PP5V_S0_KBDLED_F	6 7 40 72
	T1517	TRUE	PP5V_S3_TOPCASE_F	6 40
	T1518	TRUE	=SMB_TOPCASE_SCL	40 44
	T1519	TRUE	=SMB_TOPCASE_SDA	40 44
	T1520	TRUE	SMC_ONOFF_L	6 7 40 41 42
	T1515	TRUE	=USB2_IR_N	7 9 40
	T1522	TRUE	=USB2_IR_P	7 9 40
	T1670	TRUE	PP5V_S0_KBDLED_F	6 7 40 72
	T1735	TRUE	LSOC_H_R	6

FUNC TEST - XDP/ITP CONNECTOR

	T1693	TRUE	XDP_BPM_L<0..5>	6 10 13 66
	T1695	TRUE	NB_BSEL<0..2>	6 13 30 66
	T1696	TRUE	NB_CFG<3..8>	6 13 16
	T1681	TRUE	XDP_PWRGD	6 13
	T1683	TRUE	XDP_OBS20	6 13
	T1682	TRUE	TP_XDP_HOOK2	13
	T1684	TRUE	TP_XDP_HOOK3	13
	T1685	TRUE	LOCAL_CTRL_DATA	6 13 15
	T1687	TRUE	LOCAL_CTRL_CLK	6 13 15
	T1698	TRUE	XDP_TCK	6 10 13 66
	T1688	TRUE	SMC_WAKE_SCI_L	6 13 29 41
	T1690	TRUE	USB_EXTA_OC_L	6 13 24
	T1691	TRUE	SB_GPIO40	6 13 24
	T1692	TRUE	USB_EXTD_OC_L	6 13 24
	T1694	TRUE	WOW_EN	6 13 24 36
	T1697	TRUE	PM_LATRIGGER_L	6 13 24
	T1699	TRUE	EXTGPU_LVDS_EN	6 13 24
	T1689	TRUE	SB_GPIO30	6 13 24
	T1687	TRUE	USB_EXTB_OC_L	8 13 24
	T1700	TRUE	XDP_CLK_P	6 13 30 66 71
	T1699	TRUE	XDP_CLK_N	6 13 30 66 71
	T1701	TRUE	XDP_CPURST_L	6 13 66
	T1686	TRUE	XDP_DBRESET_L	6 10 13 28
	T1702	TRUE	XDP_TDO	6 10 13 66
	T1703	TRUE	XDP_TRST_L	6 10 13 66
	T1705	TRUE	XDP_TDI	6 10 13 66
	T1704	TRUE	XDP_TMS	6 10 13 66
	T1707	TRUE	=PP3V3_S0_XDP	8 13
	T1708	TRUE	=PP1V05_S0_XDP	8 13
x16	T1709	TRUE	GND	

FUNC TEST - RIO HATCH CONNECTOR

	T1716	TRUE	HDMI_HOST	6 37 63
	T1717	TRUE	DVI_HOST	6 37 63
	T1718	TRUE	TMDS_HTPLG	6 37 61 63
	T1719	TRUE	TMDS_DDC_SDA	6 37 61 62 63 67
	T1720	TRUE	TMDS_DDC_SCL	6 37 61 62 63 67
	T1721	TRUE	VGA_VSYNC	6 37 63
	T1722	TRUE	VGA_HSYNC	6 37 63
	T1723	TRUE	TMDS_TX_CONN_CLK_P	6 37 63 67
	T1724	TRUE	TMDS_TX_CONN_CLK_N	6 37 63 67
	T1725	TRUE	TMDS_TX_CONN_P<0..2>	6 37 63
	T1726	TRUE	TMDS_TX_CONN_N<0..2>	6 37 63
	T1727	TRUE	USB2_EXTA_F_P	6 37 39 69
	T1728	TRUE	USB2_EXTA_F_N	6 37 39 69
x14	T1729	TRUE	PP5V_S3_USB2_EXTA_F	6 37 39 72
	T1726	TRUE	PP5V_S0_DVIPORT	6 37 63 72
	T1731	TRUE	VGA_B	6 37 63 67
	T1732	TRUE	VGA_G	6 37 63 67
	T1733	TRUE	VGA_R	6 37 63 67
x14	T1710	TRUE	GND	

FUNC TEST - AIRPORT

	T1741	TRUE	CK505_SRC_CLKREQ6_L	6 7 29 36
	T1742	TRUE	PCIE_WAKE_L	6 7 25 36
	T1743	TRUE	AIRPORT_RST_L	6 7 28 36
	T1744	TRUE	=SMB_AIRPORT_CLK	36 44
	T1745	TRUE	=SMB_AIRPORT_DATA	36 44
	T1746	TRUE	GND	

NICE2HAVE NETS

FUNC TEST - Power Supplies

	T92	PPVCORE_S0_CPU	6 8 72
	T1454	PP0V9_S0	6 8 72
	T1455	PP1V05_S0	6 8 72
	T1457	PP1V25_S0	6 8 72
	T1460	PP1V5_S0	6 8 72
	T1450	PP1V8_S0	6 8 72
	T1458	PPVCORE_S0_NB_GFX	6 8 72
	T1461	PP5V_S0	6 8 72
	T1466	PP3V3_S0	72
	T1465	PP1V8_S3	6 8 72
	T1463	PP3V3_S3	6 8 72
	T1462	PP5V_S3	6 8 72
	T1467	PP3V3_S5	6 8 72
	T1468	PP5V_S5	6 8 72
	T1469	PP3V42_G3H	6 8 72
	T1472	PP18V5_G3H	6 8 72
	T1473	PPDCIN_G3H	6 8 72
	T1474	PPBUS_G3H	6 8 72
	T1475	PPBUS_R_G3H	6 8 72

FUNC TEST - M93 WIRELESS CONNECTOR

	T1476	PLT_RST_L	6 24 28
	T1479	PCIE_WAKE_L	6 7 25 36
	T1478	CK505_SRC_CLKREQ6_L	6 7 29 36
	T1476	PCIE_CLK100M_MINI_N_F	6 36
	T1475	PCIE_CLK100M_MINI_P_F	6 36
	T1476	PCIE_E_D2R_N_F	6 36
	T1477	PCIE_E_D2R_P_F	6 36
	T1480	PCIE_E_R2D_C_N_F	6 7 36
	T1483	PCIE_E_R2D_C_P_F	6 7 36
	T1484	AIRPORT_RST_L	6 7 28 36
	T1485	SMB_AIRPORT_CONN_CLK	6 36
	T1499	SMB_AIRPORT_CONN_DATA	6 36
	T1500	PCIE_E_R2D_C_N_F	6 7 36
	T1501	PCIE_E_R2D_C_P_F	6 7 36
	T1502	PP3V3_S3_AP_AUX	6 36 72

x13	T1522	GND	

Functional Test and No-Tests

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SIZE	DRAWING NUMBER	REV.
D	051-7230	J

SCALE	SHT	OF
NONE	7	109

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"S0,S0M" RAILS

(REGULATOR OUTPUT CPU VCORE PWR)

=PPVCORE_S0_CPU_REG → PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=0.9V
MAKE_BASE=TRUE

(CPU VCOR PWRE)

=PPVCORE_S0_CPU

=PP0V9_S0_REG → PP0V9_S0
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE

(DDR2 TERMINATION 0.9V PWR)

=PP0V9_S3M_MEM_TERM

(REGULATOR OUTPUT CPU 0.90V PWR)

=PP0V9_S3_VTTREF → PP0V9_S3
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE

(NB MEM VREF 0.9V PWR)

=PP0V9_S3M_MEM_NBVREFA
=PP0V9_S3M_MEM_NBVREFB
=PP0V9_S3_MEM_VREF

R0800 0 5% 1/20W MF 201
2 → 1 PP0V9_S3M_MEM_NBVREFA
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V

R0801 0 5% 1/20W MF 201
2 → 1 PP0V9_S3M_MEM_NBVREFB
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V

=PP1V05_S0_REG → PP1V05_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE

=PP1V05_S0_SB_CPU_IO
=PPVCORE_S0_SB
=PP1V05_S0_CPU
=PP1V05_S0_NB_PCIE
=PPVCORE_S0_NB
=PP1V25R1V05_S0_FSB_NB
=PP1V25R1V05_S0_NB_VTT
=PP1V05_S0M_NB_VCCAXM
=PP1V05_S0_XDP
=PP1V05_S0_SMC_LS

=PP1V25_S0_REG → PP1V25_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE

=PP1V25_S0_NB_PLL
=PP1V25_S0_NB_VCCDMI
=PP1V25_S0_SB_DMI
=PP1V25_S0_NB_VCCAXF
=PP1V25_S0_NB_VCCA
=PP1V25_S0_FET

=PP1V5_S0_REG → PP1V5_S0
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE

=PP1V5_S0_CPU
=PP1V5_S0_NB_TVDAC
=PP1V5_S0_SB
=PP1V5_S0_SB_VCC1_5_A_ARX
=PP1V5_S0_SB_VCC1_5_A_ATX
=PP1V5_S0_SB_VCC1_5_A
=PP1V5_S0_SB_VCCUSBPLL
=PP1V5_S0_SB_VCC1_5_A_USB_CORE
=PP1V5_S0_NB_FOLLOW

=PP1V8_S0_FET → PP1V8_S0
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE

=PP1V8_S0_NB_LVDS
=PP1V8_S0_NB_DPLL
=PP1V8_S0_TMDS

=PPVCORE_S0_NB_GFX_IMVP → PPVCORE_S0_NB_GFX
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE

=PPVCORE_S0_NB_GFX

=PP5V_S0_FET → PP5V_S0
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=5V
MAKE_BASE=TRUE

=PP5V_S0_SB
=PP5V_S0_LPCPLUS
=PP5V_S0_FAN
=PP5V_S0_CPU_IMVP
=PP5V_S0_NB_GFX_IMVP
=PP5V_S0_TMDS
=PP5V_S0_NB_TVDAC
=PP5V_S0_KBDLED

=PP3V3_A_S0_FET → PP3V3_A_S0
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

=PP3V3_S0_NB_VCCHV
=PP3V3_S0_NB_FOLLOW
=PP3V3_S0_SB_GPIO
=PP3V3_S0_SB_VCCGLAN3_3
=PP3V3_S0_SB_VCC3_3_PCI
=PP3V3_S0_SB_VCC3_3_IDE
=PP3V3_S0_SB_VCC3_3_VCCPCORE
=PP3V3_S0_SB_VCC3_3_SATA
=PP3V3_S0_SB_VCC3_3_DMI
=PP3V3_S0_SB
=PP3V3_S0_SB_PM
=PP3V3_S0_RSTBUF
=PP3V3_S0_LCDBKLT
=PP3V3_S0_SMBUS_SB
=PP3V3_S0_SMBUS_SMC_0_S0
=PP3V3_S0_THRM_SNR
=PP3V3_S0_XDP
=PP3V3_S0_SMC_LS
=PP3V3_S0_IMVP
=PP3V3_S0_NB_GFX_IMVP
=PP3V3_S0_PDCISENS
=PP3V3_S0MWOL_SB_VCCCL3_3
=PP3V3_S0_LCD
=PP3V3_S0_NB
=PP3V3R1V5_S0_SB_VCCHDA
=PP3V3_S0_SB_PCI
=PP3V3_S0_NB_VCCA_PEG_BG
=PP3V3_S0MWOL_SB_VCCLAN3_3
=PP3V3_S0MWOL_SB_CLINK0
=PP3V3_S0_CK505
=PP3V3_S0_NB_VCCSYNC

3V3_S0 split into 2
for layout optimization
of plane splits

=PP3V3_B_S0_FET → PP3V3_B_S0
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

3V3_B_S0 plane on right side
(peninsula)

=PP3V3_S0_TMDS
=PP3V3_S0_PATA
=PP3V3_S0_FAN
=PP3V3_S0_IDE_RESET
=PP3V3_S0_HDCP

"S3" RAILS

=PP1V8_S3_REG → PP1V8_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE

=PP1V8_S3_FET
=PP1V8_S3_MEM
=PP1V8_S3M_MEM_NB
=PP1V8_S3_NB_VCC

=PP3V3_S3_FET → PP3V3_S3
MIN_LINE_WIDTH=0.2mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=3.3V
MAKE_BASE=TRUE

=PP3V3_S3_BT
=PP3V3_S3_SMS
=PP3V3_S3_SMBUS_SMC_A_S3
=PP3V3_S3_PDCISENS
=PP3V3_S3_SMBUS_SMC_MGMT
=PP3V3_S3_SMBUS_SMC_B_S3
=PP3V3_S3_MIC
=PP3V3_S3_SMC

=PP5V_S3_FET → PP5V_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE

=PP5V_S3_CAMERA
=PP5V_S3_TOPCASE

"S5" RAILS

=PP3V3_S5_REG → PP3V3_S5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE

=PP3V3_S5_SB_PM
=PP3V3_S5_SB_USB
=PP3V3_S5_SB_GPIO
=PP3V3_S5_SB
=PP3V3_S5_FET
=PP3V3_S5_SB_VCCSUS3_3_USB
=PP3V3_S5_SB_VCCSUS3_3
=PP3V3_S5_SB_3V3_VCCSUSHDA
=PP3V3_S5_AIRPORT_AUX
=PP3V3_S5_SMBUS_SB_ME
=PP3V3_S5_ROM
=PP3V3_S5_LCD
=PP3V3_S5_SB_CLINK1
=PP3V3_S5_P1V25S0

=PP5V_S5_REG → PP5V_S5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE

=PP5V_S5_SB
=PP5V_S5_USB
=PP5V_S5_1V51V05S0
=PP5V_S5_1V8S30V9S0
=PP5V_S5_PWRCTL
=PP5V_S5_FET

"G3H" RAILS

=PP3V42_G3H_REG → PP3V42_G3H
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.42V
MAKE_BASE=TRUE

=PP3V42_G3H_SMC
=PP3V42_G3H_SMCVREF
=PP3V42_G3H_SMBUS_SMC_BSA
=PP3V42_G3H_IPD
=PP3V42_G3H_SB_RTC
=PP3V42_G3H_SMCUSBMUX
=PP3V42_G3H_CHGR
=PP3V42_G3H_LPCPLUS

=PP18V5_G3H_CHGR → PP18V5_G3H
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE

=PPDCIN_G3H → PPDCIN_G3H
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V
MAKE_BASE=TRUE

=PPVIN_G3H_P3V42G3H

=PPBUSA_G3H → PPBUS_R_G3H
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V
MAKE_BASE=TRUE

=PPVIN_S5_CPU_IMVP
=PPVIN_S5_NB_GFX_IMVP
=PPVIN_S5_1V8S30V9S0
=PPVIN_S5_1V5S0
=PPVIN_S5_1V05S0

=PPBUSB_G3H → PPBUS_G3H
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V
MAKE_BASE=TRUE

=PPVIN_S5_5VS5
=PPVIN_S5_3V3S5
=PPVIN_S0_LCDBKLT
=PPVIN_S0_AUDIO
=PPVIN_G3H_DCIN

Power Aliases

SYNC_MASTER=WFERRY
SYNC_DATE=06/15/2006

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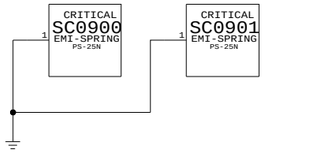
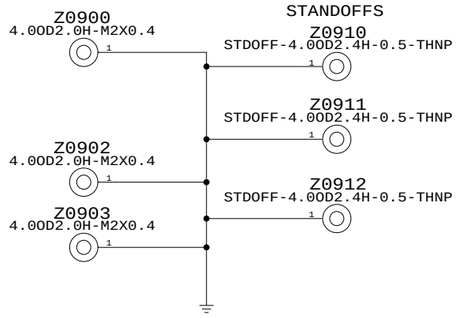
EMI SPRING CLIPS

PLACE CLIPS PER MCO ON TOPSIDE NEAR BATTERY CONNECTOR J6900



BOSSES TO CONNECT TO HEATSINK



SMC ALIASES

NO-CONNECT UNUSED SMC INTERFACE PORTS

			NO_TEST
41	SMC_PA0	NC_SMC_PA0	TRUE
41	SMC_PA1	NC_SMC_PA1	TRUE
41	SMC_PB0	NC_SMC_PB0	TRUE
41	SMC_PG0	NC_SMC_PG0	TRUE
41	SMC_P14	NC_SMC_P14	TRUE
41	SMC_P20	NC_SMC_P20	TRUE
41	SMC_P21	NC_SMC_P21	TRUE
41	SMC_P22	NC_SMC_P22	TRUE
41	SMC_P23	NC_SMC_P23	TRUE
41	SMC_P26	NC_SMC_P26	TRUE
41	SMC_P27	NC_SMC_P27	TRUE
41	SMC_P41	NC_SMC_P41	TRUE
41	SMC_P43	NC_SMC_P43	TRUE
41	SMC_P44	NC_SMC_P44	TRUE
41	SMC_P46	NC_SMC_P46	TRUE
41	SMC_P62	NC_SMC_P62	TRUE
41	SMC_P63	NC_SMC_P63	TRUE
41	SMC_P64	NC_SMC_P64	TRUE
41	SMC_P67	NC_SMC_P67	TRUE
41	SMC_P81	NC_SMC_P81	TRUE
41	SMC_GFX_OVERTEMP_L	NC_SMC_GFX_OVERTEMP_L	TRUE
41	SMC_EXCARD_OC_L	NC_EXCARD_OC_L	TRUE
41	SMC_BATT_TRICKLE_EN_L	NC_SMC_BATT_TRICKLE_EN_L	TRUE
41	SMC_EXCARD_CP	NC_SMC_EXCARD_CP	TRUE
41	SMC_P45	NC_SMC_ENRGYSTR_LDO_EN	TRUE
41	SMC_PH4	NC_SMC_ENRGYSTR_LDO_PGOOD	TRUE
41	ALS_RIGHT	NC_ALS_RIGHT	TRUE
41	ALS_GAIN	NC_ALS_GAIN	TRUE
41	SMC_EXCARD_PWR_EN	NC_SMC_EXCARD_PWR_EN	TRUE
41	SMC_FAN_1_CTL	NC_SMC_FAN_1_CTL	TRUE
41	SMC_FAN_2_CTL	NC_SMC_FAN_2_CTL	TRUE
41	SMC_FAN_3_CTL	NC_SMC_FAN_3_CTL	TRUE
41	SMC_FAN_1_TACH	NC_SMC_FAN_1_TACH	TRUE
41	SMC_FAN_2_TACH	NC_SMC_FAN_2_TACH	TRUE
41	SMC_FAN_3_TACH	NC_SMC_FAN_3_TACH	TRUE
41	SMC_PF0	NC_SMC_PF0	TRUE
41	SMC_BATT_VSET	NC_SMC_BATT_VSET	TRUE
41	SMC_SYS_VSET	NC_SMC_SYS_VSET	TRUE
41	SMC_RSTGATE_L	NC_SMC_RSTGATE_L	TRUE
41	SMC_GFX_THROTTLE_L	NC_SMC_GFX_THROTTLE_L	TRUE
41	SMC_SYS_ISET	NC_SYS_ISET	TRUE
41	SMC_BATT_ISET	NC_BATT_ISET	TRUE
41	ISENSE_CAL_EN	NC_ISENSE_CAL_EN	TRUE
41	SMC_FWE	NC_SMC_FWE	TRUE
41	SMC_ANALOG_ID	NC_SMC_ANALOG_ID	TRUE
41	SMC_TEST_DAC1	NC_SMC_TEST_DAC1	TRUE
41	SMC_TEST_DAC2	NC_SMC_TEST_DAC2	TRUE
41	SMC_TEST_DAC3	NC_SMC_TEST_DAC3	TRUE

48 6 SMC_SMS_INT — =SMC_SMS_INT 41

42 41 6 SMC_ADAPTER_EN — SMC_ADAPTER_PRESENT 36

LVDS ALIASES

NO-CONNECT UNUSED LVDS INTERFACE PORTS

			NO_TEST
67 15	LVDS_B_CLK_N	NC_LVDS_B_CLK_N	TRUE
67 15	LVDS_B_CLK_P	NC_LVDS_B_CLK_P	TRUE
67 15	LVDS_B_DATA_N<0>	NC_LVDS_B_DATA_N0	TRUE
67 15	LVDS_B_DATA_N<1>	NC_LVDS_B_DATA_N1	TRUE
67 15	LVDS_B_DATA_N<2>	NC_LVDS_B_DATA_N2	TRUE
67	LVDS_B_DATA_N<3>	NC_LVDS_B_DATA_N3	TRUE
67 15	LVDS_B_DATA_P<0>	NC_LVDS_B_DATA_P0	TRUE
67 15	LVDS_B_DATA_P<1>	NC_LVDS_B_DATA_P1	TRUE
67 15	LVDS_B_DATA_P<2>	NC_LVDS_B_DATA_P2	TRUE
67	LVDS_B_DATA_P<3>	NC_LVDS_B_DATA_P3	TRUE
67	LVDS_A_DATA_P<3>	NC_LVDS_A_DATA_P3	TRUE
67	LVDS_A_DATA_N<3>	NC_LVDS_A_DATA_N3	TRUE

PCI_EXPRESS GRAPHICS ALIASES

NO-CONNECT UNUSED SDVO INTERFACE PORTS

67 15	PEG_D2R_N<0>	NC_PEG_D2R_N0	TRUE
67 15	PEG_D2R_N<2>	NC_PEG_D2R_N2	TRUE
67 15	PEG_D2R_N<3>	NC_PEG_D2R_N3	TRUE
67 15	PEG_D2R_N<4>	NC_PEG_D2R_N4	TRUE
67 15	PEG_D2R_N<5>	NC_PEG_D2R_N5	TRUE
67 15	PEG_D2R_N<6>	NC_PEG_D2R_N6	TRUE
67 15	PEG_D2R_N<7>	NC_PEG_D2R_N7	TRUE
67 15	PEG_D2R_N<8>	NC_PEG_D2R_N8	TRUE
67 15	PEG_D2R_N<9>	NC_PEG_D2R_N9	TRUE
67 15	PEG_D2R_N<10>	NC_PEG_D2R_N10	TRUE
67 15	PEG_D2R_N<11>	NC_PEG_D2R_N11	TRUE
67 15	PEG_D2R_N<12>	NC_PEG_D2R_N12	TRUE
67 15	PEG_D2R_N<13>	NC_PEG_D2R_N13	TRUE
67 15	PEG_D2R_N<14>	NC_PEG_D2R_N14	TRUE
67 15	PEG_D2R_N<15>	NC_PEG_D2R_N15	TRUE
67 15	PEG_D2R_P<0>	NC_PEG_D2R_P0	TRUE
67 15	PEG_D2R_P<2>	NC_PEG_D2R_P2	TRUE
67 15	PEG_D2R_P<3>	NC_PEG_D2R_P3	TRUE
67 15	PEG_D2R_P<4>	NC_PEG_D2R_P4	TRUE
67 15	PEG_D2R_P<5>	NC_PEG_D2R_P5	TRUE
67 15	PEG_D2R_P<6>	NC_PEG_D2R_P6	TRUE
67 15	PEG_D2R_P<7>	NC_PEG_D2R_P7	TRUE
67 15	PEG_D2R_P<8>	NC_PEG_D2R_P8	TRUE
67 15	PEG_D2R_P<9>	NC_PEG_D2R_P9	TRUE
67 15	PEG_D2R_P<10>	NC_PEG_D2R_P10	TRUE
67 15	PEG_D2R_P<11>	NC_PEG_D2R_P11	TRUE
67 15	PEG_D2R_P<12>	NC_PEG_D2R_P12	TRUE
67 15	PEG_D2R_P<13>	NC_PEG_D2R_P13	TRUE
67 15	PEG_D2R_P<14>	NC_PEG_D2R_P14	TRUE
67 15	PEG_D2R_P<15>	NC_PEG_D2R_P15	TRUE
67 15	PEG_R2D_C_N<4>	NC_PEG_R2D_C_N4	TRUE
67 15	PEG_R2D_C_N<5>	NC_PEG_R2D_C_N5	TRUE
67 15	PEG_R2D_C_N<6>	NC_PEG_R2D_C_N6	TRUE
67 15	PEG_R2D_C_N<7>	NC_PEG_R2D_C_N7	TRUE
67 15	PEG_R2D_C_N<8>	NC_PEG_R2D_C_N8	TRUE
67 15	PEG_R2D_C_N<9>	NC_PEG_R2D_C_N9	TRUE
67 15	PEG_R2D_C_N<10>	NC_PEG_R2D_C_N10	TRUE
67 15	PEG_R2D_C_N<11>	NC_PEG_R2D_C_N11	TRUE
67 15	PEG_R2D_C_N<12>	NC_PEG_R2D_C_N12	TRUE
67 15	PEG_R2D_C_N<13>	NC_PEG_R2D_C_N13	TRUE
67 15	PEG_R2D_C_N<14>	NC_PEG_R2D_C_N14	TRUE
67 15	PEG_R2D_C_N<15>	NC_PEG_R2D_C_N15	TRUE
67 15	PEG_R2D_C_P<4>	NC_PEG_R2D_C_P4	TRUE
67 15	PEG_R2D_C_P<5>	NC_PEG_R2D_C_P5	TRUE
67 15	PEG_R2D_C_P<6>	NC_PEG_R2D_C_P6	TRUE
67 15	PEG_R2D_C_P<7>	NC_PEG_R2D_C_P7	TRUE
67 15	PEG_R2D_C_P<8>	NC_PEG_R2D_C_P8	TRUE
67 15	PEG_R2D_C_P<9>	NC_PEG_R2D_C_P9	TRUE
67 15	PEG_R2D_C_P<10>	NC_PEG_R2D_C_P10	TRUE
67 15	PEG_R2D_C_P<11>	NC_PEG_R2D_C_P11	TRUE
67 15	PEG_R2D_C_P<12>	NC_PEG_R2D_C_P12	TRUE
67 15	PEG_R2D_C_P<13>	NC_PEG_R2D_C_P13	TRUE
67 15	PEG_R2D_C_P<14>	NC_PEG_R2D_C_P14	TRUE
67 15	PEG_R2D_C_P<15>	NC_PEG_R2D_C_P15	TRUE

GND
VOLTAGE=0V
MIN_NECK_WIDTH=0.20 MM
MIN_LINE_WIDTH=0.38 MM

SATA ALIASES

NO-CONNECT UNUSED SATA INTERFACE PORTS

69	SATA_A_D2R_N	NC_SATA_A_D2R_N	TRUE
69	SATA_A_D2R_P	NC_SATA_A_D2R_P	TRUE
69 23	SATA_A_R2D_C_N	NC_SATA_A_R2D_C_N	TRUE
69 23	SATA_A_R2D_C_P	NC_SATA_A_R2D_C_P	TRUE
69	SATA_B_D2R_N	NC_SATA_B_D2R_N	TRUE
69	SATA_B_D2R_P	NC_SATA_B_D2R_P	TRUE
69 23	SATA_B_R2D_C_N	NC_SATA_B_R2D_C_N	TRUE
69 23	SATA_B_R2D_C_P	NC_SATA_B_R2D_C_P	TRUE
69	SATA_C_D2R_N	NC_SATA_C_D2R_N	TRUE
69	SATA_C_D2R_P	NC_SATA_C_D2R_P	TRUE
69 23	SATA_C_R2D_C_N	NC_SATA_C_R2D_C_N	TRUE
69 23	SATA_C_R2D_C_P	NC_SATA_C_R2D_C_P	TRUE

CLOCK ALIASES

NO-CONNECT UNUSED CLOCK INTERFACE PORTS

29	TP_CK505_SRC1_N	NC_CK505_SRC1_N	TRUE
29	TP_CK505_SRC1_P	NC_CK505_SRC1_P	TRUE
29	TP_CK505_SRC_CLKREQ1_L	NC_CK505_SRC_CLKREQ1_L	TRUE
29	TP_CK505_SRC3_N	NC_CK505_SRC3_N	TRUE
29	TP_CK505_SRC3_P	NC_CK505_SRC3_P	TRUE
29	TP_CK505_SRC_CLKREQ3_L	NC_CK505_SRC_CLKREQ3_L	TRUE
29	TP_CK505_SRC4_N	NC_CK505_SRC4_N	TRUE
29	TP_CK505_SRC4_P	NC_CK505_SRC4_P	TRUE
29	TP_CK505_SRC_CLKREQ4_L	NC_CK505_SRC_CLKREQ4_L	TRUE
29	TP_CK505_SRC7_N	NC_CK505_SRC7_N	TRUE
29	TP_CK505_SRC7_P	NC_CK505_SRC7_P	TRUE
29	TP_CK505_PGMODE	NC_CK505_PGMODE	TRUE
29	TP_CK505_SRC8_N	NC_CK505_SRC8_N	TRUE
29	TP_CK505_SRC8_P	NC_CK505_SRC8_P	TRUE
29	TP_CK505_SRC_CLKREQ8_L	NC_CK505_SRC_CLKREQ8_L	TRUE
29	TP_GPU_STOP_L	NC_GPU_STOP_L	TRUE
29	TP_CK505_PCI1_CLK	NC_CK505_PCI1_CLK	TRUE
29	TP_CK505_PCI2_CLK	NC_CK505_PCI2_CLK	TRUE
29	TP_CK505_PCI4_CLK	NC_CK505_PCI4_CLK	TRUE

SB ALIASES

NO-CONNECT UNUSED INTERFACE PORTS

25	VR_PWRGD_CLKEN	VR_PWRGD_CK505	6 28
25	=SB_CLINK_MPWROK	PM_SB_PWROK	6 25 28
70 24	PCI_AD<0..31>	NC_PCI_AD<0..31>	TRUE
70 24	PCI_C_BE_L<0..3>	NC_PCI_C_BE_L<0..3>	TRUE
70 24	PCI_PAR	NC_PCI_PAR	TRUE
24	PCI_RST_L	TP_PCI_RST_L	6

NB ALIASES

16	=GFX_VR_EN	GFX_VR_EN	6 53
16	=NB_CLINK_MPWROK	VR_PWRGOOD_DELAY	6 16 28 52
16	=NB_CLK96M_DOT_P	NB_CLK96M_DOT_P	6 30 71
16	=NB_CLK96M_DOT_N	NB_CLK96M_DOT_N	6 30 71
16	=NB_CLK100M_DPLLSS_P	NB_CLK100M_DPLLSS_P	6 30 71
16	=NB_CLK100M_DPLLSS_N	NB_CLK100M_DPLLSS_N	6 30 71
15	LVDS_BKLT_CTL	LCDBKLT_PWM_UNBUF	6 64
15	LVDS_BKLT_EN	LCDBKLT_PWREN	6 64

AUDIO ALIASES

37 7	HDA_BITCLK	HDA_BIT_CLK	6 23 69
69 37 23 9 7 6	HDA_SYNC	HDA_SYNC	6 7 9 23 37 69
69 37 23 9 6	HDA_RST_L	HDA_RST_L	6 9 23 37 69
37 7	HDA_SDATAIN0	HDA_SDIN0	6 23 69
37 7	HDA_SDATAOUT	HDA_SDOUT	6 23 69

USB ALIASES

USB PORT [0] = External USB2.0 Port A

39	=USB2_EXTA_P 6	USB2_EXTA_P	USB_EXTA_P 24 69
39	=USB2_EXTA_N 6	USB2_EXTA_N	USB_EXTA_N 24 69
39	=EXTAUSB_OC_L 6	EXTAUSB_OC_L	USB_EXTA_OC_L 7 13 24
	39 6	USB2_MUXED_EXTA_N	USB_EXTA_MUXED_P 69
	39 6	USB2_MUXED_EXTA_P	USB_EXTA_MUXED_N 69

USB PORT [1] = PCI-E Mini Card

36	=USB2_AIRPORT_P 6	USB2_AIRPORT_P	USB_MINI_P 24 69
36	=USB2_AIRPORT_N 6	USB2_AIRPORT_N	USB_MINI_N 24 69

USB PORT [2] = Unused

	=USB2_3G_P	TP_USB2_3G_P	USB_EXTD_P 24 69
	=USB2_3G_N	TP_USB2_3G_N	USB_EXTD_N 24 69

USB PORT [3] = CAMERA

60	=USB2_CAMERA_P 6	USB2_CAMERA_P	USB_CAMERA_P 24 69
60	=USB2_CAMERA_N 6	USB2_CAMERA_N	USB_CAMERA_N 24 69

USB PORT [4] = IR CONTROLLER

40 7	=USB2_IR_P 69 24 9 6	USB_IR_P	USB_IR_P 6 9 24 69
40 7	=USB2_IR_N 69 24 9 6	USB_IR_N	USB_IR_N 6 9 24 69

USB PORT [5] = Trackpad(Wellspring)

40 7	=USB2_TRACKPAD_P 6	USB2_WSPRING_P	USB_TPAD_P 24 69
40 7	=USB2_TRACKPAD_N 6	USB2_WSPRING_N	USB_TPAD_N 24 69

USB PORT [6] = BLUETOOTH

	=USB2_BT_P	NC_USB_BT_P	USB_BT_P 24 69
	=USB2_BT_N	NC_USB_BT_N	USB_BT_N 24 69

USB PORT [7] = Unused

	NC_USB2_EXTB_P		USB_EXTB_P 24 69
	NC_USB2_EXTB_N		USB_EXTB_N 24 69
	=EXTBUSB_OC_L 6	EXTBUSB_OC_L	USB_EXTB_OC_L 7 13 24

USB PORT [8] = Unused

TP_USB_EXCARD_P		USB_EXCARD_P 24 69
TP_USB_EXCARD_N		USB_EXCARD_N 24 69

USB PORT [9] = Unused

TP_USB_EXTC_P		USB_EXTC_P 24 69
TP_USB_EXTC_N		USB_EXTC_N 24 69

SIGNAL ALIAS /RESET

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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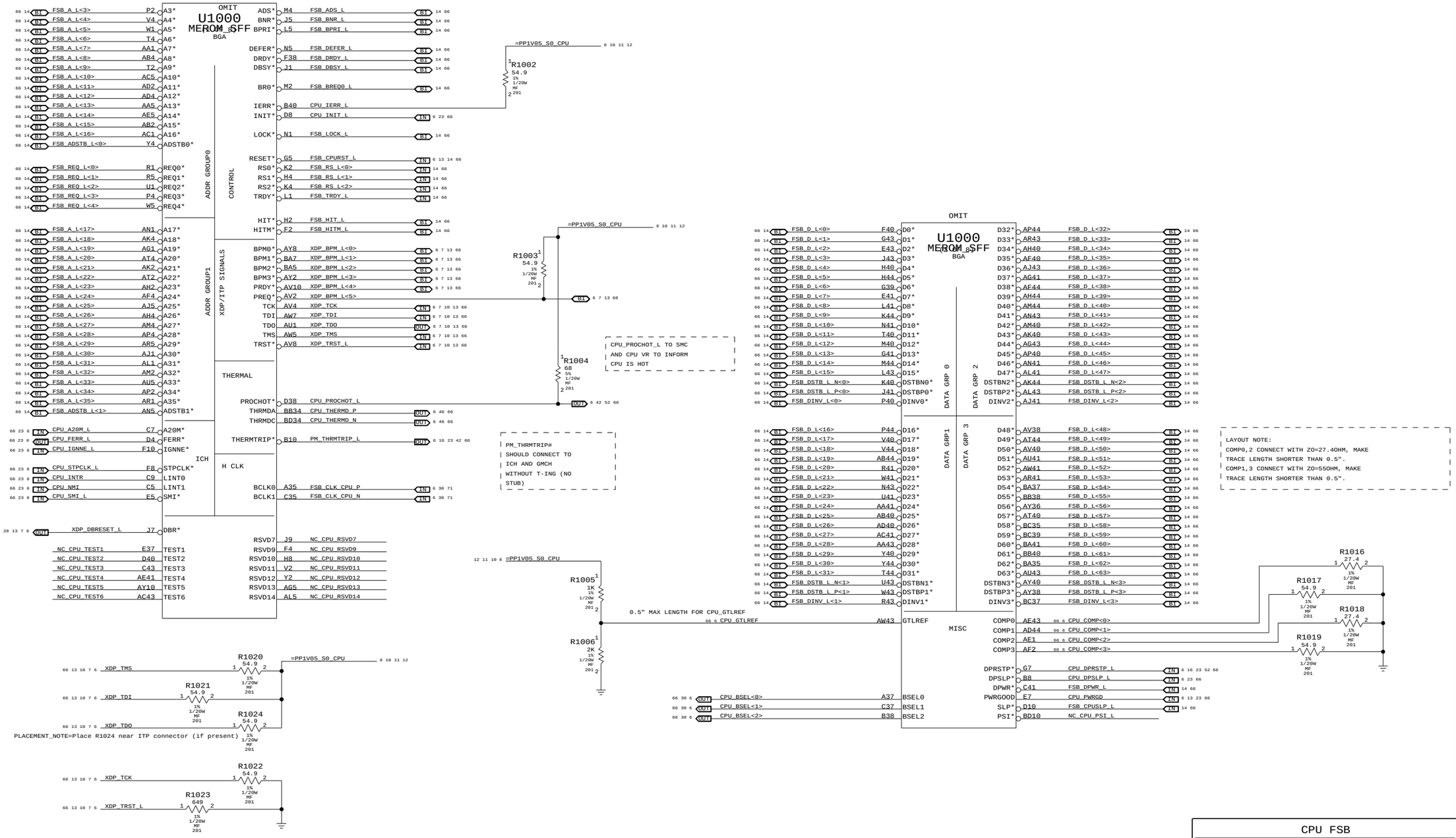

CPU FSB

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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=PPVCORE_S0_CPU 65 12 11 8

=PPVCORE_S0_CPU 8 11 12 65

(CPU CORE POWER) 29A

U1000 MEROM_SFF (3 OF 8) OMIT BGA

VCC: H32 G33 F32 N33 M32 L33 K32 J33 W33 V32 U33 T32 R33 P32 AD32 AC33 AB32 AA33 Y32 AK32 AJ33 AH32 AG33 AF32 AE33 AR33 AP32 AN33 AM32 AL33 AY32 AV32 AU33 AT32 AT34 BD32 BB32 B26 B30 B28 H26 F26 D26 H28 H30 F28 F30 D30 D28 M26 K26 M28 M30 K28 K30 V26 T26 P26 V28 V30 T28 T30 P28 P30 AD26 AB26 Y26

VCC: AD28 AD30 AB28 AB30 Y28 Y30 AK26 AH26 AF26 AK28 AK30 AH28 AH30 AF28 AF30 AP26 AM26 AP28 AP30 AM28 AM30 AY26 AV26 AT26 AY28 AY30 AV28 AV30 AT28 AT30 BD26 BB26 BD28

(CPU IO POWER 1.05V) 2.5A

=PP1V05_S0_CPU 8 10 11 12

VCCP: N37 L37 K38 J37 W37 V38 U37 R37 P38 AC37 AB38 AA37 AK38 AJ37 AG37 AF38

(CPU INTERNAL PLL POWER 1.5V) 0.130A

VCCA=1.5 ONLY

=PP1V5_S0_CPU 8 12

VCCA: B34 D34

VID:

BD8	CPU_VID<0>	OUT 6 12 52 66
BC7	CPU_VID<1>	OUT 6 12 52 66
BB10	CPU_VID<2>	OUT 6 12 52 66
BB8	CPU_VID<3>	OUT 6 12 52 66
BC5	CPU_VID<4>	OUT 6 12 52 66
BB4	CPU_VID<5>	OUT 6 12 52 66
AY4	CPU_VID<6>	OUT 6 12 52 66

VCCSENSE BD12

VSSSENSE BC13

=PPVCORE_S0_CPU 8 11 12 65

R1100 100 1% 1/20W MF 201

CPU_VCCSENSE_P OUT 6 52 66

CPU_VCCSENSE_N OUT 6 52 66

R1101 100 1% 1/20W MF 201

LAYOUT NOTE:
CPU_VCCSENSE_P/CPU_VCCSENSE_N USE
ZO=27.4 OHM DIFFERENTIAL TRACE ROUTING.

LAYOUT NOTE:
PLACE R1100 AND R1101
WITHIN 1 INCH OF CPU W/ NO STUB

LAYOUT NOTE:
PROVIDE A TEST POINT (WITH NO STUB)
TO CONNECT A DIFFERENTIAL PROBE
BETWEEN VCCSENSE AND VSSSENSE

(7 OF 8) OMIT U1000 MEROM_SFF BGA

VCC: BD30 BB28 BB30 B24 B22 H22 H24 F22 F24 D24 D22 M22 M24 K22 K24 V22 V24 T22 T24 P22 P24 AD22 AD24 AB22 AB24 Y22 Y24 AK22 AK24 AH22 AH24 AF22 AF24 AP22 AP24 AM22 AM24 AY22 AY24 AV22 AV24 AT22 AT24 BD22 BD24 BB22 BB24 B20 B18 B16 H20 F20 D20 H16 H18 F16 F18 D18 D16 M20

VCC: K20 M16 M18 K16 K18 V20 T20 P20 V16 V18 T16 T18 P16 P18 AD20 AB20 Y20 AD16 AD18 AB16 AB18 Y16 Y18 AK20 AK16 AK18 AH20 AF20 AH16 AH18 AF16 AF18 AP20 AM20 AP16 AP18 AM16 AM18 AY20 AV20 AT20 AY16 AY18 AV16 AV18 AT16 AT18 BD20 BB20 BD16 BD18 BB16 BB18 AP14 AM14 AY14 AV14 AT14 BD14 BB14

(8 OF 8) OMIT U1000 MEROM_SFF BGA

VCCP: AE37 AP38 AN37 AL37 C33 B32 H36 F36 G35 F34 E33 E35 D32 K36 N35 L35 J35 W35 V36 P36 U35 R35 AB36 AC35 AA35 AK36 AF36 AJ35 AG35 AE35 AP36 AN35 AL35 C13 B14 B12 H12 H14 G11 G13 F12 F14 E11 E13 D14 D12 K10 N11 N13 M14 L11 L13 K12 K14 J11 J13 V10 P10 W11 W13 V12 V14 U11 U13 T14 R11

=PP1V05_S0_CPU 8 10 11 12

VCCP: R13 P12 P14 AB10 AD14 AC11 AC13 AB12 AB14 AA11 AA13 Y14 AK10 AF10 AK12 AK14 AJ11 AJ13 AH14 AG11 AG13 AF12 AF14 AE11 AE13 AP10 AR11 AR13 AP12 AN11 AN13 AL11 AL13 AU11 AU13 N7 N9 L7 L9 W7 W9 U7 U9 R7 R9 AC7 AC9 AA7 AA9 AJ7 AJ9 AG7 AG9 AE7 AE9 AR7 AR9 AN7 AN9 AL7 AL9 A33 A13

(6 OF 8) OMIT U1000 MEROM_SFF BGA

VSS: Y6 Y8 AK6 AK8 AH6 AH8 AF6 AF8 AP6 AP8 AM6 AM8 AY6 AW9 AU7 AV6 AU9 AT6 AT8 BD6 BC9 BB6 BA9 C3 B4 G3 E3 D2 N3 L3 J3 W3 U3 R3 AC3 AA3

VSS: AJ3 AG3 AE3 AR3 AN3 AL3 AW3 AU3 BD4 BC3 BB2 BA3 G1 E1 AW1 BA1 A39 A41 A31 A27 A29 A21 A23 A25 A17 A19 A15 A11 A9 A5 A7

(4 OF 8) OMIT U1000 MEROM_SFF BGA

VSS: B42 H42 F42 D42 D44 F44 M42 K42 V42 T42 P42 AD42 AB42 Y42 AK42 AH42 AF42 AP42 AM42 AY42 AV42 AT42 AV44 AY44 BB42 BA43 C39 H38 G37 E39 N39 M38 L39 J39 W39 U39 T38 R39 AD38 AC39 AA39 Y38 AJ39 AH38 AG39 AE39 AR37 AR39 AN39 AM38 AL39 AW37 AW39 AU37 AU39 AT38 BD38 BD40 BC41 BA39 B36 D36 H34 M36 M34 K34 T36 V34 T34 P34 AD36 Y36 AD34 AB34 Y34 AK34 AH36 AH34 AF34 AR35 AM36

VSS: AP34 AM34 AV36 AT36 AY34 AW33 AW35 AV34 AU35 BD36 BB36 BC33 BA33 C31 C29 C27 G31 E31 G27 G29 E27 E29 N31 L31 J31 N27 N29 L27 L29 J27 J29 W31 W27 W29 U31 R31 U27 U29 R27 R29 AC31 AA31 AC27 AC29 AA27 AA29 AJ31 AG31 AE31 AJ27 AJ29 AG27 AG29 AE27 AE29 AR31 AR27 AR29 AN31 AL31 AN27 AN29 AL27 AL29 AW31 AU31 AW27 AW29 AU27 AU29 BC31 BA31 BC27 BC29 BA27 BA29 C25 C23 C21 G21 G23 G25

(5 OF 8) OMIT U1000 MEROM_SFF BGA

VSS: E21 E23 E25 N21 N23 N25 L21 L23 L25 J21 J23 J25 W21 W23 W25 U21 U23 U25 R21 R23 R25 AC21 AC23 AC25 AA21 AA23 AA25 AJ21 AJ23 AJ25 AG21 AG23 AG25 AE21 AE23 AE25 AR21 AR23 AR25 AN21 AN23 AN25 AL21 AL23 AL25 AW21 AW23 AW25 AU21 AU23 AU25 BC21 BC23 BC25 BA21 BA23 BA25 C19 C17 G17 G19 E17 E19 N17 N19 L17 L19 J17 J19 W17 W19 U17 U19 R17 R19 AC17 AC19 AA17 AA19 AJ17 AJ19 AG17 AG19

VSS: AE17 AE19 AR17 AR19 AN17 AN19 AL17 AL19 AW17 AW19 AU17 AU19 BC17 BC19 BA17 BA19 C15 C11 H10 G15 E15 M10 N15 L15 J15 M12 T10 W15 U15 R15 T12 AD10 Y10 AC15 AA15 AD12 Y12 AH10 AJ15 AG15 AE15 AH12 AM10 AR15 AN15 AL15 AM12 AT10 AW15 AU15 AY12 AW11 AW13 AV12 AT12 BC15 BA15 BC11 BB12 BA11 BA13 B6 H6 G9 F6 E9 D6 M6 M8 K6 K8 U5 V6 V8 T6 T8 P6 P8 AD6 AD8 AB6 AB8

CPU Power & Ground

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE	SHT	OF
NONE	11	109

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CPU VCORE HF AND BULK DECOUPLING

3x 330uF. 32x 10uF 0603, 28x 1uF 0402

Intel recommends 32+28 but is evaluating 24+24

65 11 8 =PPVCORE_S0_CPU

10UF 0603 = APN:138S0568 = MURATA,TAIYO,TDK,SAMSUNG

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C1200 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1201 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1202 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1203 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1204 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1205 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1206 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1207 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1208 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1209 10UF 20% 6.3V X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C1210 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1211 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1212 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1213 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1214 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1215 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1216 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1217 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1218 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1219 10UF 20% 6.3V X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITIICAL C1220 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1221 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1222 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1223 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1224 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1225 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1226 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1227 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1228 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1229 10UF 20% 6.3V X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C1230 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1231 10UF 20% 6.3V X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C1240 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1241 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1242 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1243 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1244 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1245 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1246 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1247 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1248 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1249 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C1250 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1251 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1252 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1253 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1254 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1255 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1256 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1257 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1258 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1259 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C1260 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1261 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1262 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1263 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1264 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1265 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1266 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1267 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON SAME SIDE AS CPU

CRITICAL C1270 330UF 20% 2.0V TANT D2T
CRITICAL C1271 330UF 20% 2.0V TANT D2T

CRITICAL C1272 330UF 20% 2.0V TANT D2T

LAYOUT NOTE:
PLACE ON SAME SIDE AS CPU

Intel recommends 3x220UF @ 9mOHM

CPU VCORE VID CONNECTIONS

66 52 11 6 CPU_VID<0..6> (MAKE_BASE=TRUE) —— IMVP6_VID<0..6> 66

VCCA (CPU AVdd) DECOUPLING

11 8 =PP1V5_S0_CPU

1x 10uF, 1x 0.01uF

OMIT C1280 10uF 20% 6.3V X5R 603
C1281 0.01UF 10% 10V X5R 201

LAYOUT NOTE:
PLACE C1281 NEAR PIN B34 OF U1000

VCCP (CPU I/O) DECOUPLING

11 10 8 =PP1V05_S0_CPU

1X 330UF, 12X 2.2UF

OMIT C1283 2.2UF 20% 6.3V CERM 402-LF
OMIT C1284 2.2UF 20% 6.3V CERM 402-LF
OMIT C1285 2.2UF 20% 6.3V CERM 402-LF
OMIT C1286 2.2UF 20% 6.3V CERM 402-LF
OMIT C1287 2.2UF 20% 6.3V CERM 402-LF
OMIT C1288 2.2UF 20% 6.3V CERM 402-LF

CRITICAL C1290 330UF 20% 2.5V POLY CASE-C2-SM-1

OMIT C1291 2.2UF 20% 6.3V CERM 402-LF
OMIT C1292 2.2UF 20% 6.3V CERM 402-LF
OMIT C1293 2.2UF 20% 6.3V CERM 402-LF
OMIT C1294 2.2UF 20% 6.3V CERM 402-LF
OMIT C1295 2.2UF 20% 6.3V CERM 402-LF
OMIT C1296 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE C1290 CLOSE TO CPU
PLACE C1283-C1288 CLOSE TO FSB ADDRESS PINS
PLACE C1291-C1296 CLOSE TO FSB DATA PINS

CPU Decoupling & VID

SYNC_MASTER=MSARWAR SYNC_DATE=04/26/2006

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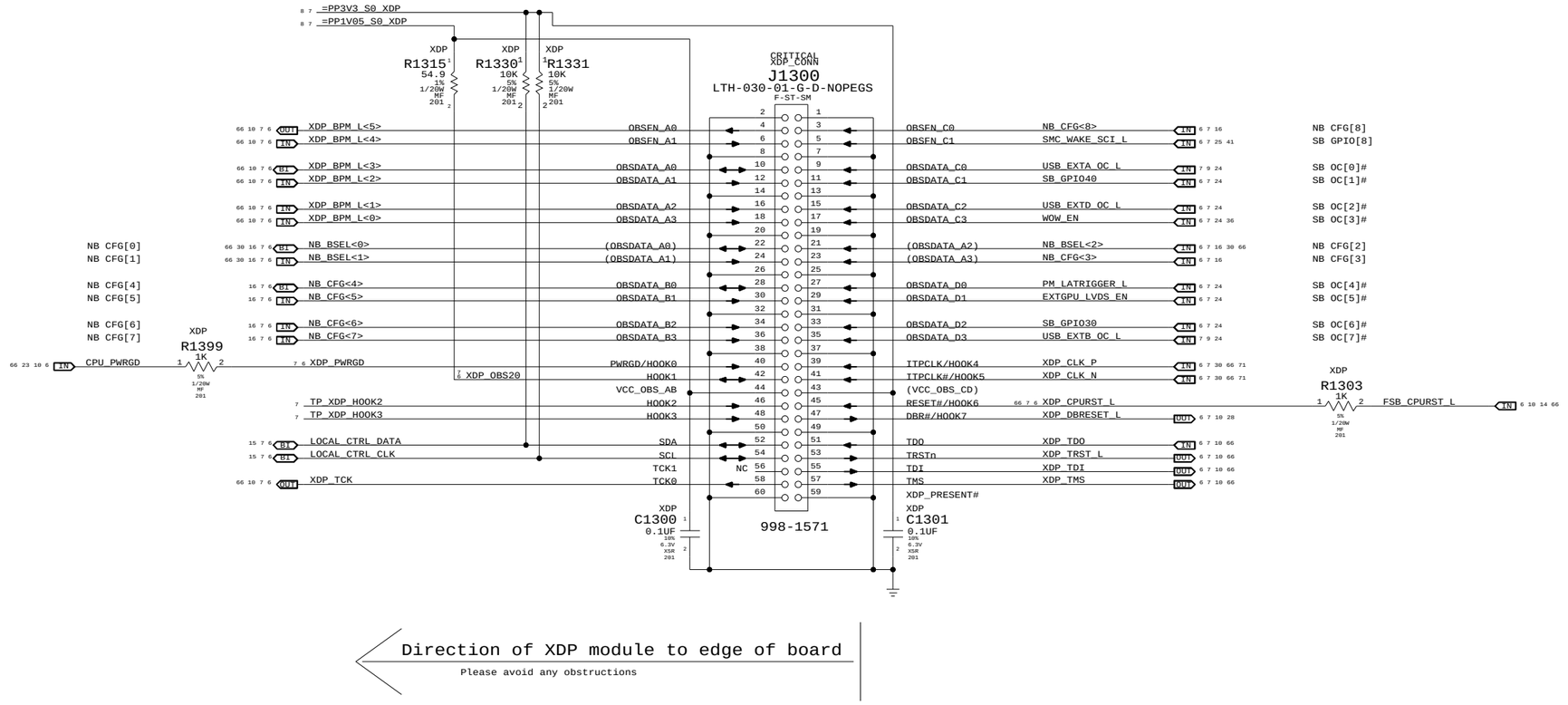
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0451 adapter board to support CPU, NB & SB debugging.



Direction of XDP module to edge of board

Please avoid any obstructions

eXtended Debug Port (XDP)

SYNC_MASTER=M75 SYNC_DATE=01/24/2007

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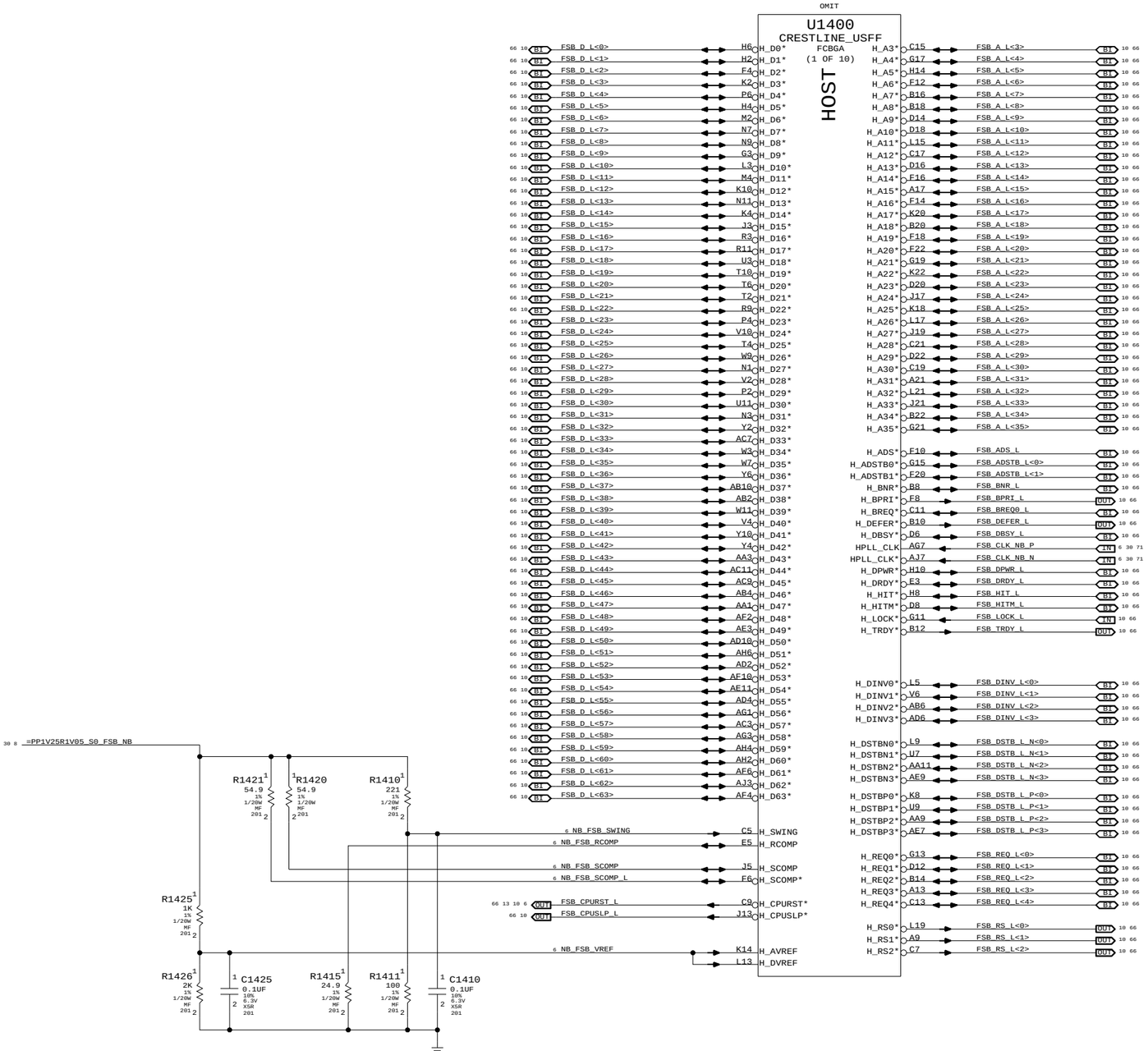

NB CPU Interface

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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NONE	14	109

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LVDS Disable

Can leave all signals NC if LVDS is not implemented.
Tie VCC_TX_LVDS and VCCA_LVDS to GND.

If SDVO is used, VCCD_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable / CRT Enable

Tie TVx_DAC and TVx_RTN to GND. Must power all TVDAC rails. VCCA_TVx_DAC and VCCA_DAC_BG can share filtering with VCCA_CRT_DAC.

CRT Disable / TV-Out Enable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND. All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA_CRT.

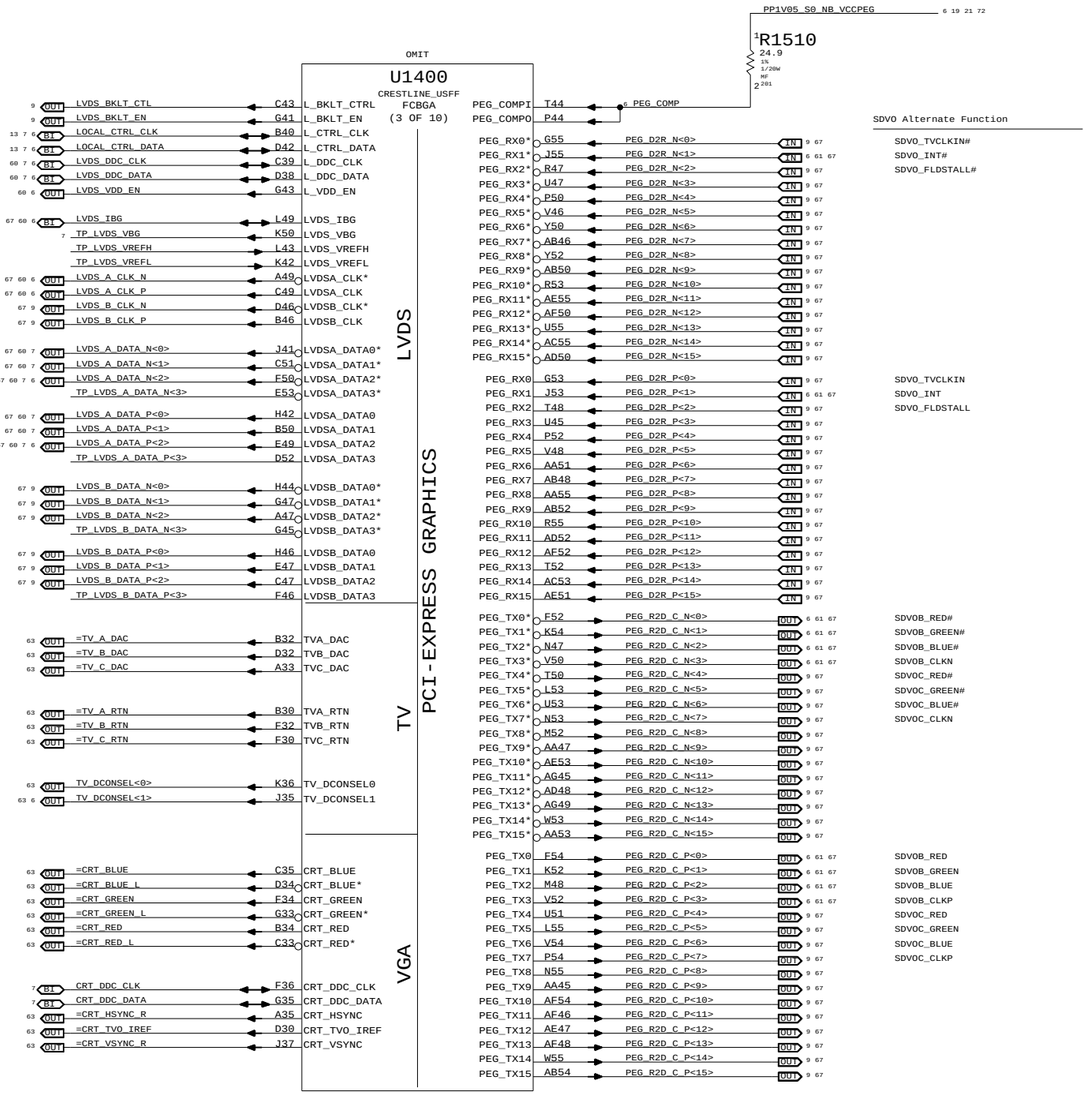
CRT & TV-Out Disable

Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT_TVO_IREF to GND.
Can tie the following rails to GND:
VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC, VCCD_CRT, VCCD_QDAC and VCC_SYNC.

NOTE: Must keep VDDC_TVDAC powered and filtered at all times!

Internal Graphics Disable

Follow instructions for LVDS and CRT & TV-Out Disable above.
Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and TV_DCONSELx to GND.
Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.
Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).
Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore).
Tie VCC_AXG and VCC_AXG_NCTF to GND.
Leave GFX_VID<3..0> and GFX_VR_EN as NC.



NB PEG / Video Interfaces

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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NB_CFG<3>	RESERVED
NB_CFG<4>	RESERVED
NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2
NB_CFG<6>	RESERVED
NB_CFG<7>	RESERVED
NB_CFG<8>	RESERVED
NB_CFG<9> PCIe Graphics Lane Reversal	High = Normal Low = Reversed
NB_CFG<10>	RESERVED
NB_CFG<11>	RESERVED
NB_CFG<12>	See Below
NB_CFG<13>	See Below
NB_CFG<14>	RESERVED
NB_CFG<15>	RESERVED
NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled
NB_CFG<17>	RESERVED
NB_CFG<18>	RESERVED
NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal
NB_CFG<20> Concurrent SDVO/PCIe x1	High = Both active Low = Only SDVO or PCIe x16

NB_CFG<13:12>

00 = RESERVED
01 = XOR Mode Enabled
10 = All-Z Mode Enabled
11 = Normal Operation

NB CFG<5> chooses DMI x4 w/ TP

NB_CFG<9> 6 16
NBCFG_PEG_REVERSE
R1659 4.02K 1% 1/20W MF 201

NB_CFG<16> 6 16
NBCFG_DYN_ODT_DISABLE
R1666 4.02K 1% 1/20W MF 201

=PP3V3_S0_NB_VCCHV 8 16 19 21 22
NBCFG_DMI_REVERSE
R1669 4.02K 1% 1/20W MF 201
NB_CFG<19> 6 16

=PP3V3_S0_NB_VCCHV 8 16 19 21 22
NBCFG_SDVO_AND_PCIE
R1670 4.02K 1% 1/20W MF 201
NB_CFG<20> 6 16

NB CFG<8:0> used for debug access

NB CFG<13:12> require ICT access

22 21 19 16 8 =PP3V3_S0_NB_VCCHV
R1630 10K 5% 1/20W MF 201
R1631 10K 5% 1/20W MF 201
41 6 IN PM_EXTTS_L<0>
41 6 IN PM_EXTTS_L<1>

OMIT

U1400
CRESTLINE_USFF
FCBGA
(2 OF 10)

RSVD bit ordering based on CRB numbering

TP_NB_RSVD<42>	A39	RSVD
7 TP_NB_RSVD<8>	AG11	RSVD
7 TP_NB_RSVD<7>	AG9	RSVD
7 TP_NB_RSVD<5>	AH10	RSVD
7 TP_NB_RSVD<6>	AJ11	RSVD
TP_NB_RSVD<12>	AJ43	RSVD
TP_NB_RSVD<11>	AL43	RSVD
TP_NB_RSVD<13>	AN43	RSVD
TP_NB_RSVD<10>	AR43	RSVD
TP_NB_RSVD<45>	B36	RSVD
TP_NB_RSVD<41>	B38	RSVD
7 TP_NB_RSVD<21>	B55	RSVD
7 TP_NB_RSVD<28>	BA33	RSVD
7 TP_NB_RSVD<35>	BB22	RSVD
7 TP_NB_RSVD<29>	BC33	RSVD
7 TP_NB_RSVD<30>	BF22	RSVD
7 TP_NB_RSVD<31>	BE23	RSVD
7 TP_NB_RSVD<24>	BH18	RSVD
7 TP_NB_RSVD<36>	BE27	RSVD
7 TP_NB_RSVD<22>	BJ17	RSVD
7 TP_NB_RSVD<25>	BK16	RSVD
7 TP_NB_RSVD<27>	BK18	RSVD
7 TP_NB_RSVD<34>	BK32	RSVD
7 TP_NB_RSVD<26>	BL17	RSVD
7 TP_NB_RSVD<23>	BL19	RSVD
TP_NB_RSVD<43>	C37	RSVD
TP_NB_RSVD<9>	D10	RSVD
TP_NB_RSVD<44>	D36	RSVD
7 TP_NB_RSVD<4>	G51	RSVD
TP_NB_RSVD<20>	G9	RSVD
7 TP_NB_RSVD<3>	H52	RSVD
7 TP_NB_RSVD<14>	J25	RSVD
7 TP_NB_RSVD<1>	M46	RSVD
7 TP_NB_RSVD<2>	N45	RSVD

DDR MUXING

SM_CK0	BC37	MEM_CLK_P<0>	OUT 31 33 68
SM_CK1	BC25	MEM_CLK_P<1>	OUT 31 33 68
SM_CK3	BB36	MEM_CLK_P<3>	OUT 32 33 68
SM_CK4	BB24	MEM_CLK_P<4>	OUT 32 33 68
SM_CK0*	BA37	MEM_CLK_N<0>	OUT 31 33 68
SM_CK1*	BC23	MEM_CLK_N<1>	OUT 31 33 68
SM_CK3*	BB34	MEM_CLK_N<3>	OUT 32 33 68
SM_CK4*	BB26	MEM_CLK_N<4>	OUT 32 33 68
SM_CKE0	BE33	MEM_CKE<0>	OUT 31 33 68
SM_CKE1	BE35	MEM_CKE<1>	OUT 31 33 68
SM_CKE3	BF40	MEM_CKE<3>	OUT 32 33 68
SM_CKE4	BE39	MEM_CKE<4>	OUT 32 33 68
SM_CS0*	BA23	MEM_CS_L<0>	OUT 31 33 68
SM_CS1*	BH16	MEM_CS_L<1>	OUT 31 33 68
SM_CS2*	BE15	MEM_CS_L<2>	OUT 32 33 68
SM_CS3*	BH14	MEM_CS_L<3>	OUT 32 33 68
SM_ODT0	BJ15	MEM_ODT<0>	OUT 6 31 33 68
SM_ODT1	BF20	MEM_ODT<1>	OUT 6 31 33 68
SM_ODT2	BE13	MEM_ODT<2>	OUT 6 32 33 68
SM_ODT3	BH12	MEM_ODT<3>	OUT 6 32 33 68
SM_RCOMP	BL13	6 MEM_RCOMP	
SM_RCOMP*	BK14	6 MEM_RCOMP_L	
SM_RCOMP_VOH	BK36	6 MEM_RCOMP_VOH	
SM_RCOMP_VOL	BL37	6 MEM_RCOMP_VOL	
SM_VREF0	AM54	PP0V9_S3M_MEM_NBVREFA	IN 8 21 68
SM_VREF1	AT12	PP0V9_S3M_MEM_NBVREFB	IN 8 21 68

68 21 18 8 =PP1V8_S3M_MEM_NB

R1610 20 1% 1/20W MF 201
R1620 1K 1% 1/20W MF 201
C1623 0.01UF 10% 10V X5R 201
OMIT C1622 2.2UF 20% 6.3V CERM 402-LF
R1622 3.01K 1% 1/20W MF 201
C1615 0.1UF 10% 6.3V X5R 201
C1616 0.1UF 10% 6.3V X5R 201
R1611 20 1% 1/20W MF 201
C1625 0.01UF 10% 10V X5R 201
OMIT C1624 2.2UF 20% 6.3V CERM 402-LF
R1624 1K 1% 1/20W MF 201

CLK

DPLL_REF_CLK	C45	=NB_CLK96M_DOT_P	IN 9
DPLL_REF_CLK*	B44	=NB_CLK96M_DOT_N	IN 9
DPLL_REF_SSCLK	H50	=NB_CLK100M_DPLLSS_P	IN 9
DPLL_REF_SSCLK*	G49	=NB_CLK100M_DPLLSS_N	IN 9
PEG_CLK	N51	NB_CLK100M_PCIE_P	IN 6 30 71
PEG_CLK*	M50	NB_CLK100M_PCIE_N	IN 6 30 71

Clk used for PEG and DMI

CFG

66 30 13 7 6 IN NB_BSEL<0>	H28	CFG0	
66 30 13 7 6 IN NB_BSEL<1>	G25	CFG1	
66 30 13 7 6 IN NB_BSEL<2>	C25	CFG2	
13 7 6 OUT NB_CFG<3>	K24	CFG3	IPU
13 7 6 BI NB_CFG<4>	B28	CFG4	IPU
13 7 6 BI NB_CFG<5>	G27	CFG5	IPU
13 7 6 OUT NB_CFG<6>	B26	CFG6	IPU
13 7 6 OUT NB_CFG<7>	D26	CFG7	IPU
13 7 6 OUT NB_CFG<8>	D24	CFG8	IPU
16 6 NB_CFG<9>	F26	CFG9	IPU
7 TP_NB_CFG<10>	A25	CFG10	IPU
7 TP_NB_CFG<11>	L23	CFG11	IPU
TP_NB_CFG<12>	D28	CFG12	IPU
TP_NB_CFG<13>	F24	CFG13	IPU
7 TP_NB_CFG<14>	C29	CFG14	IPU
7 TP_NB_CFG<15>	C27	CFG15	IPU
16 6 NB_CFG<16>	A29	CFG16	IPU
7 TP_NB_CFG<17>	J27	CFG17	IPU
TP_NB_CFG<18>	G31	CFG18	IPD
16 6 NB_CFG<19>	K30	CFG19	IPD
16 6 NB_CFG<20>	L37	CFG20	IPD

DMI

DMI_RXN0	AL45	DMI_S2N_N<0>	IN 6 24 67
DMI_RXN1	AK54	DMI_S2N_N<1>	IN 6 24 67
DMI_RXN2	AJ55	DMI_S2N_N<2>	IN 6 24 67
DMI_RXN3	AH52	DMI_S2N_N<3>	IN 6 24 67
DMI_RXP0	AM46	DMI_S2N_P<0>	IN 6 24 67
DMI_RXP1	AK52	DMI_S2N_P<1>	IN 6 24 67
DMI_RXP2	AJ53	DMI_S2N_P<2>	IN 6 24 67
DMI_RXP3	AH50	DMI_S2N_P<3>	IN 6 24 67
DMI_TXN0	AH48	DMI_N2S_N<0>	OUT 6 24 67
DMI_TXN1	AK48	DMI_N2S_N<1>	OUT 6 24 67
DMI_TXN2	AG55	DMI_N2S_N<2>	OUT 6 24 67
DMI_TXN3	AL53	DMI_N2S_N<3>	OUT 6 24 67
DMI_TXP0	AJ47	DMI_N2S_P<0>	OUT 6 24 67
DMI_TXP1	AK50	DMI_N2S_P<1>	OUT 6 24 67
DMI_TXP2	AG53	DMI_N2S_P<2>	OUT 6 24 67
DMI_TXP3	AL55	DMI_N2S_P<3>	OUT 6 24 67

PM

25 6 OUT PM_BMBUSY_L	F44	PM_BM_BUSY*	
66 52 23 10 6 IN CPU_DPRSTP_L	C41	PM_DPRSTP*	
	L38	PM_EXT_TS0*	
	J39	PM_EXT_TS1*	
52 28 9 6 IN VR_PWRGOOD_DELAY	AT50	PWROK	
28 6 IN NB_RESET_L	BB20	RSTIN*	
66 42 23 10 6 OUT PM_THRMTRIP_L	F28	THERMTRIP*	
66 52 25 6 IN PM_DPRSLPVR	F40	DPRSLPVR	

GRAPHICS VID

		GFX_VID<4>	OUT 53
GFX_VID0	G37	GFX_VID<0>	OUT 6 22 53
GFX_VID1	A45	GFX_VID<1>	OUT 6 22 53
GFX_VID2	B42	GFX_VID<2>	OUT 6 22 53
GFX_VID3	D44	GFX_VID<3>	OUT 6 22 53
GFX_VR_EN	F42	=GFX_VR_EN	OUT 9

ME

CL_CLK	BE52	CLINK_NB_CLK	BI 6 25 70
CL_DATA	BE53	CLINK_NB_DATA	BI 6 25 70
CL_PWROK	AP50	=NB_CLINK_MPWROK	IN 9
CL_RST*	BH52	CLINK_NB_RESET_L	OUT 6 25 70
CL_VREF	BE54	70 6 NB_CLINK_VREF	

NC

7 TP_NB_NC<14>	A52	NC
7 TP_NB_NC<13>	A54	NC
7 TP_NB_NC<12>	B54	NC
7 TP_NB_NC<10>	BH1	NC
7 TP_NB_NC<2>	BH55	NC
7 TP_NB_NC<9>	BK1	NC
7 TP_NB_NC<8>	BK2	NC
7 TP_NB_NC<4>	BK54	NC
7 TP_NB_NC<1>	BK55	NC
7 TP_NB_NC<7>	BL2	NC
7 TP_NB_NC<6>	BL4	NC
7 TP_NB_NC<5>	BL52	NC
7 TP_NB_NC<3>	BL54	NC
7 TP_NB_NC<11>	D55	NC

MISC

SDVO_CTRL_CLK	K38	SDVO_CTRLCLK	BI 6 61
SDVO_CTRL_DATA	K40	SDVO_CTRLDATA	BI 6 61
CLKREQ*	G39	NB_CLKREQ_L	OUT 6 29
ICH_SYNC*	D40	NB_SB_SYNC_L	OUT 6 25
TEST1	F38	6 NB_TEST1	
TEST2	K34	6 NB_TEST2	

R1691 20K 5% 1/20W MF 201
R1690 0 5% 1/20W MF 201

PP1V25_S0M_NB_VCCAXD 19 21
R1640 1K 1% 1/20W MF 201
C1640 0.1UF 10% 6.3V X5R 201
R1641 392 1% 1/20W MF 201

NOTE: GMCH CL_PWROK input must be PWRGD signal for PP3V3_S0M, PP3V3_S0MWOL, PP1V8_S3M, PP1V25_S0M, PP1V05_S0M, PP0V9_S3M and PP0V9_S0M.
If ME/AMT is not used, short CL_PWROK to PWROK.

NB Misc Interfaces

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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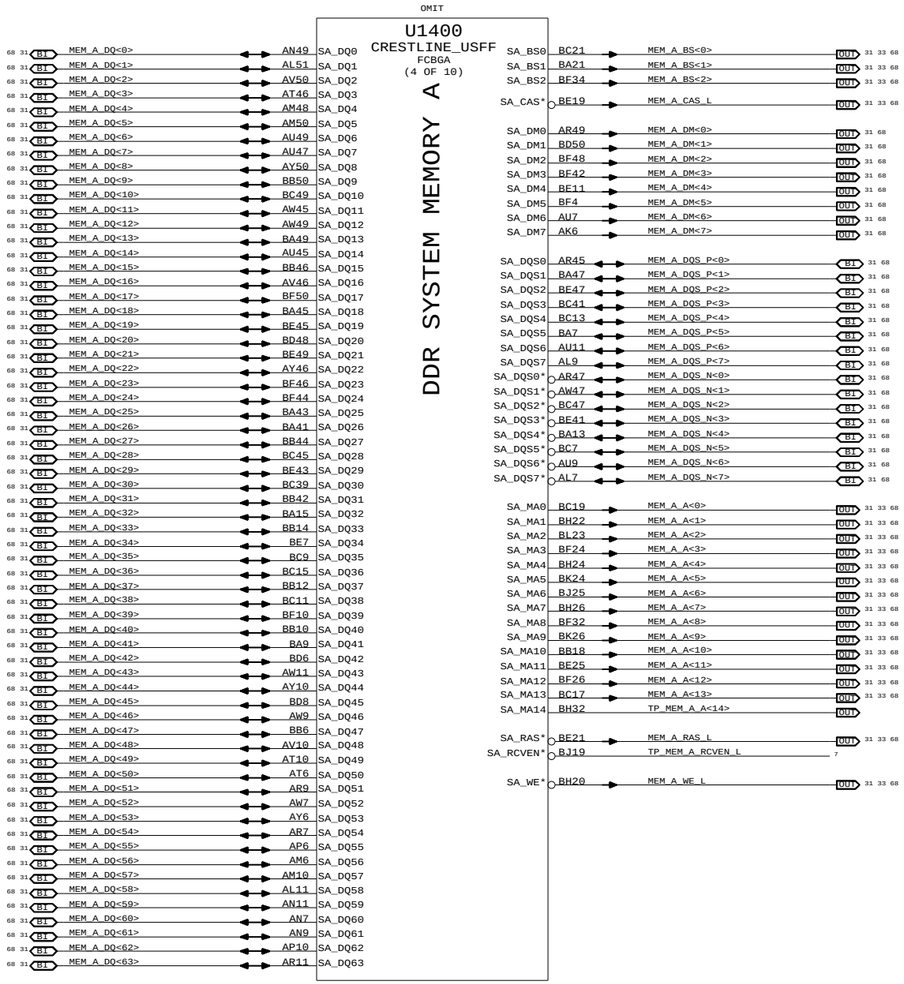

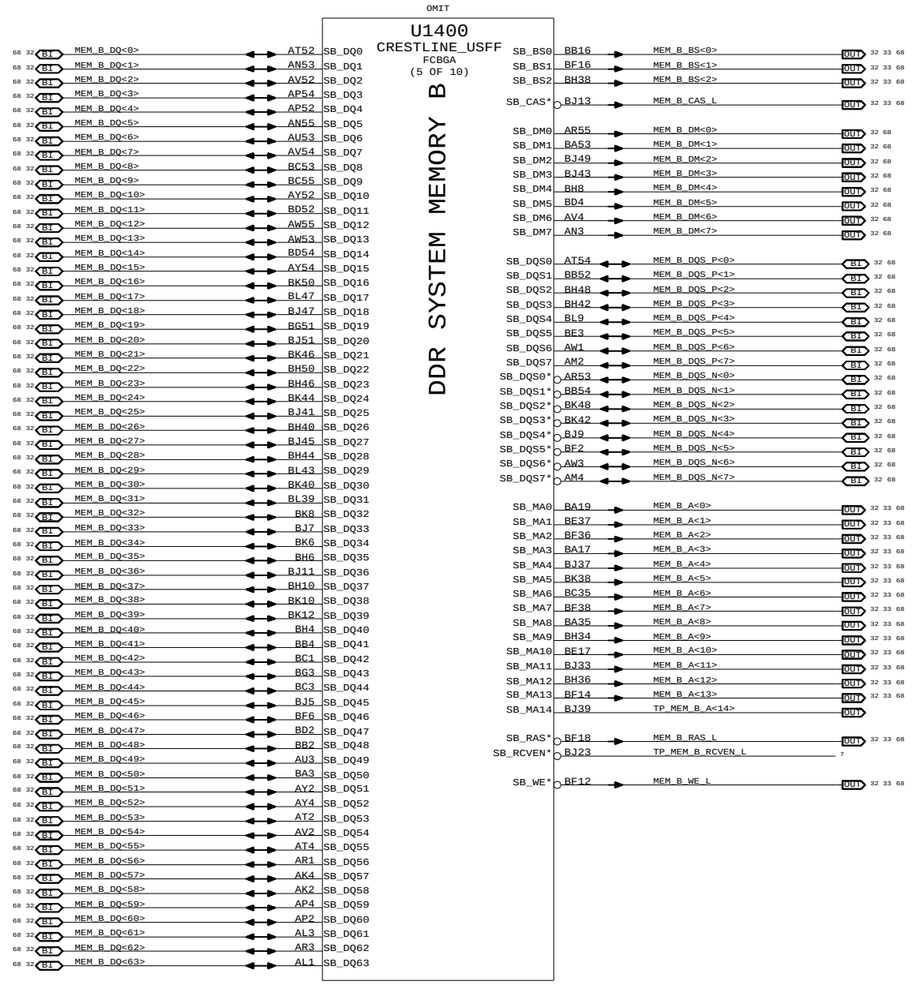

NB DDR2 Interfaces

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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NCTF balls are Not Critical To Function

These connections can break without impacting part performance.

=PPVCORE_S0_NB_GFX 8 18 22 53 65

=PPVCORE_S0_NB 21 18 8

1310 mA (Ext Graphics)
1600 mA (Int Graphics)

=PPVCORE_S0_NB_GFX 8 18 22 53 65

7700 mA (Int Graphics)

=PP1V8_S3M_MEM_NB 68 21 16 8

3300 mA (2 ch, 667MHz)
2700 mA (2 ch, 533MHz)
1700 mA (1 ch, 667MHz)
1395 mA (1 ch, 533MHz)
5 mA (standby)

NB_VCCSM_LF1 68 6
NB_VCCSM_LF2 68 6
NB_VCCSM_LF3 68 6
NB_VCCSM_LF4 68 6
NB_VCCSM_LF5 68 6
NB_VCCSM_LF6 68 6
NB_VCCSM_LF7 68 6

C1807 0.1UF 10% 6.3V X5R 201
C1806 0.1UF 10% 6.3V X5R 201
C1805 0.22UF 20% 6.3V X5R 402
C1804 0.22UF 20% 6.3V X5R 402
C1803 0.47UF 10% 6.3V CERM-X5R 402
C1802 1uF OMIT 10% 6.3V CERM 402
C1801 1uF OMIT 10% 6.3V CERM 402

=PP1V25_S0M_NB_VCCA_SM 21
640mA

=PPVCORE_S0_NB 21 18 8

540mA

=PP1V05_S0M_NB_VCCAXM 21 18 8

=PP1V05_S0M_NB_VCCAXM 21 18 8

POWER
OMIT
(6 OF 10)
U1400
FCBGA
CRESTLINE_USFF

POWER
OMIT
(7 OF 10)
U1400
FCBGA
CRESTLINE_USFF

Current numbers from Crestline EDS, doc #21749.

NB Power 1	
SYNC_MASTER=M70	SYNC_DATE=01/09/2007

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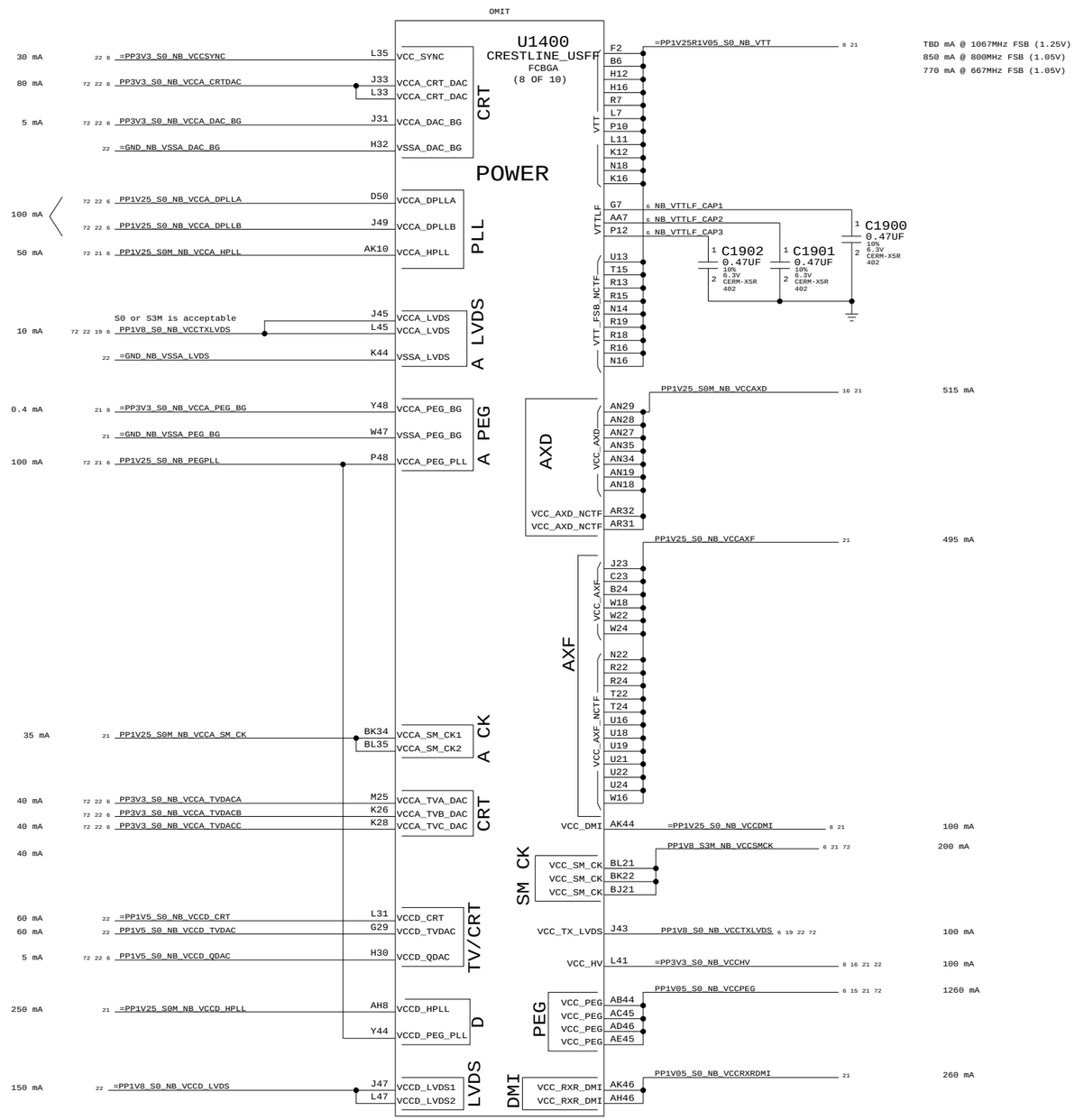

Current numbers from Crestline EDS, doc #21749.

NB Power 2

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SIZE D | DRAWING NUMBER 051-7230 | REV. J

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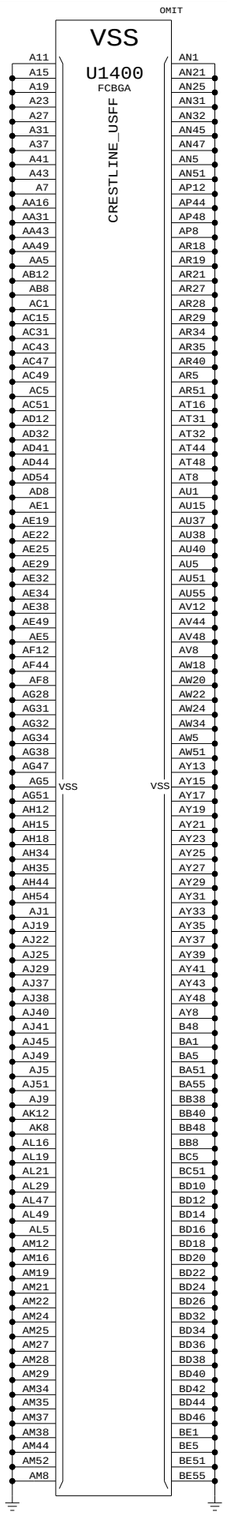

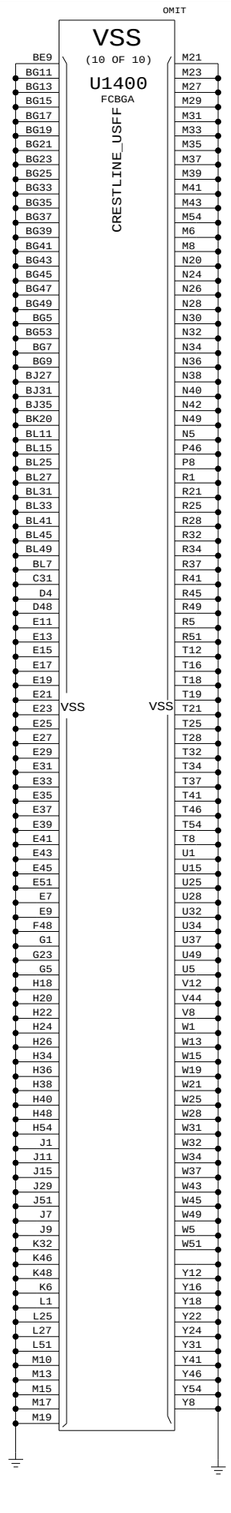

NB Grounds

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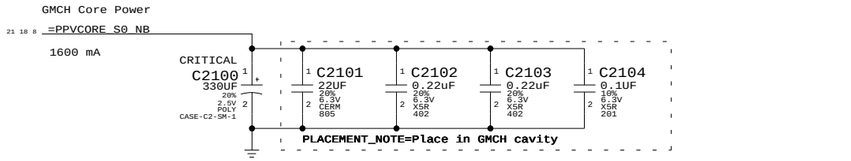

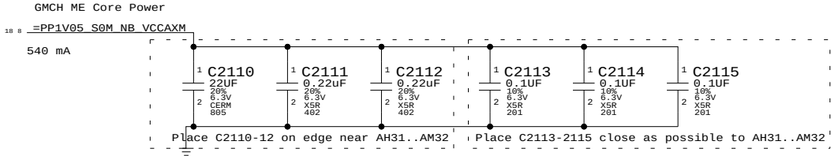

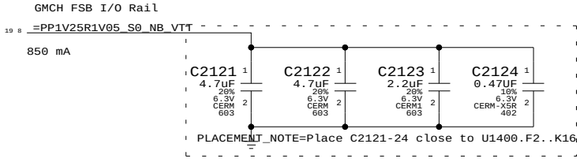

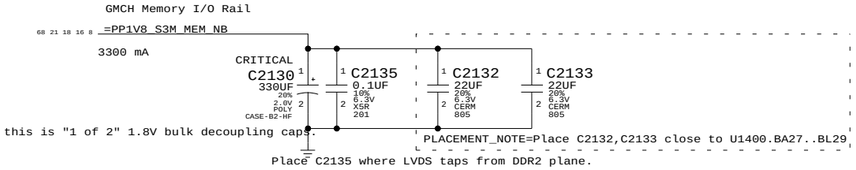

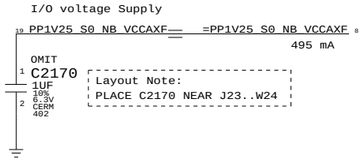

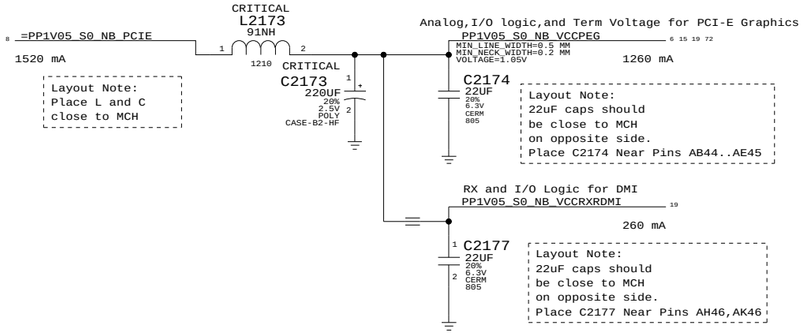

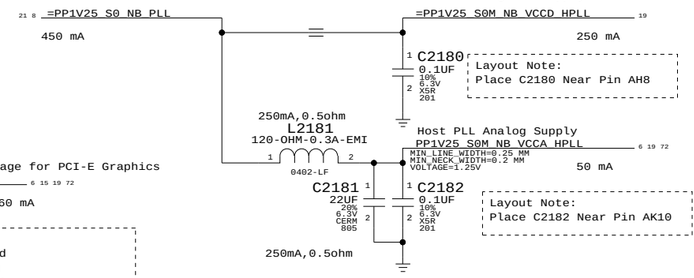

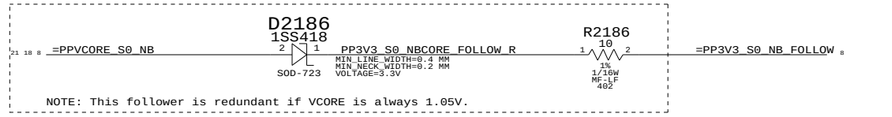

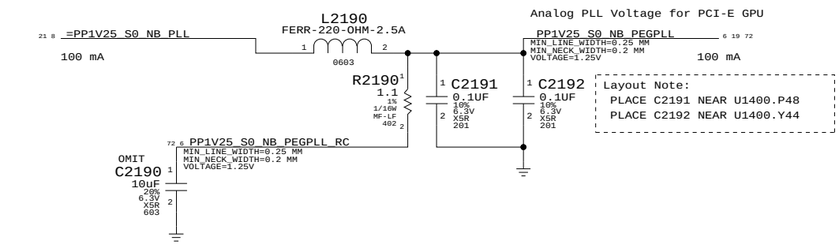

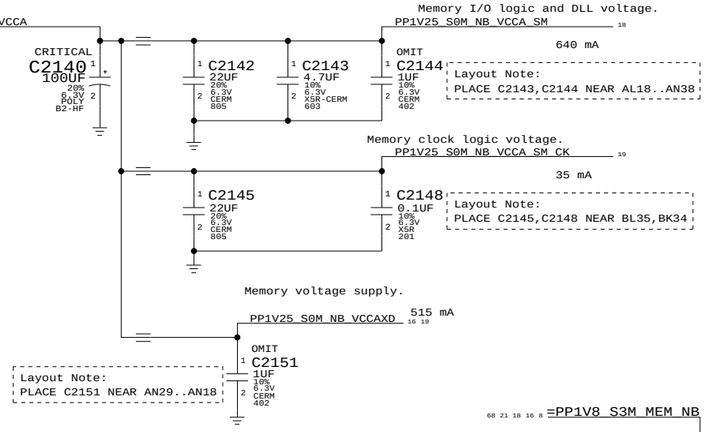

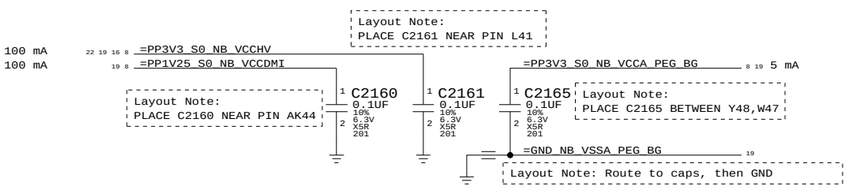

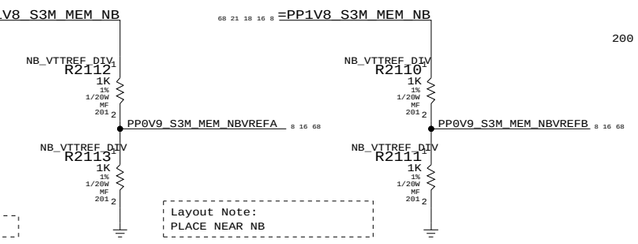

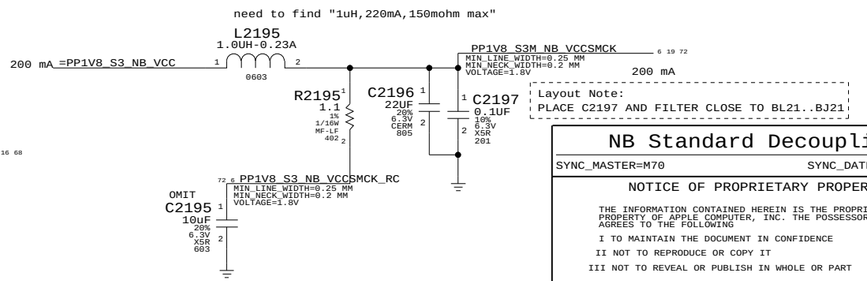

Current numbers from Crestline EDS Addendum, doc .....

NB Standard Decoupling

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NOTE: This filter is required even if using only external graphics.

VCCD_TVDAC also powers internal thermal sensors.

=PP1V5_S0_NB_TVDAC
125 mA
CRITICAL C2201 22000pF-1000mA 16V NFM18
C2202 0.01UF 10% 10V X5R 201
C2200 0.1UF 10% 6.3V X5R 201
PP1V5_S0_NB_VCCD_TVDAC
MIN_LINE_WIDTH=0.2 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.5V
60 mA
PP1V5_S0_NB_VCCD_CRT
MIN_LINE_WIDTH=0.2 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.5V
60 mA
=PP1V5_S0_NB_VCCD_CRT
PP1V5_S0_NB_VCCD_CRT MAKE_BASE=TRUE

R2205 100 1% 1/10W MF-LF 402
PP1V5_S0_NB_QDAC
MIN_LINE_WIDTH=0.2 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.5V
C2205 0.01UF 10% 10V X5R 201
CRITICAL C2206 22000pF-1000mA 16V NFM18
C2207 0.1UF 10% 6.3V X5R 201
C2208 1UF 10% 10V X5R 402-1
PP1V5_S0_NB_VCCD_QDAC
MIN_LINE_WIDTH=0.2 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.5V
500 uA

Filtering changed per SR MOW # 541194

Layout Note:
These 4 caps should be
within 6.35 mm of NB edge

=PP5V_S0_NB_TVDAC
205 mA
OMIT C2280 1UF 10% 6.3V CERM 402
R2281 0 5% 1/20W MF 201
NO STUFF C2281 1UF 10% 6.3V CERM 402
=P3V3TVDAC_EN_RC
U2280 TPS79933 SON
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=3.3V
IN OUT EN NR NC GND THRML PAD
PP3V3_S0_NB_TVDAC
205 mA
P3V3TVDAC_NOISE
C2282 0.01UF 10% 10V X5R 201
OMIT C2285 10UF 20% 6.3V CERM 603

CRITICAL L2288 180-OHM-1.5A 0603
PP3V3_S0_NB_CRTDAC_F
MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=3.3V
80 mA
C2295 0.01UF 10% 10V X5R 201
C2288 0.1UF 10% 6.3V X5R 201
CRITICAL C2289 22000pF-1000mA 16V NFM18
PP3V3_S0_NB_VCCA_CRTDAC
MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=3.3V
80 mA

Layout Note:
These 2 caps should be
within 6.35 mm of NB edge

NO STUFF D2285 1SS418 SOD-723
=PP1V5_S0_NB_FOLLOW
PP3V3_S0_NB_TVDAC_FOLLOW
MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=3.3V
NO STUFF R2285 10 1% 1/10W MF-LF 402

CRITICAL L2290 180-OHM-1.5A 0603
PP3V3_S0_NB_TVDAC_F
MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=3.3V
125 mA
C2293 0.01UF 10% 10V X5R 201
C2291 0.1UF 10% 6.3V X5R 201
CRITICAL C2292 22000pF-1000mA 16V NFM18
PP3V3_S0_NB_VCCA_TVDACA
MIN_LINE_WIDTH=0.3 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=3.3V
40 mA
CRITICAL C2294 22000pF-1000mA 16V NFM18
PP3V3_S0_NB_VCCA_TVDACB
MIN_LINE_WIDTH=0.3 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=3.3V
40 mA

Layout Note:
These 11 caps should be
within 6.35 mm of NB edge

CRITICAL C2296 22000pF-1000mA 16V NFM18
PP3V3_S0_NB_VCCA_TVDACC
MIN_LINE_WIDTH=0.3 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=3.3V
40 mA

GMCH Graphics Core Power
=PPVCORE_S0_NB_GFX
7700 mA
CRITICAL C2210 330UF 20% 2.5V POLY CASE-C2-SM-1
OMIT C2219 10uF 20% 6.3V X5R 603
OMIT C2231 10uF 20% 6.3V X5R 603
OMIT C2232 10uF 20% 6.3V X5R 603
OMIT C2240 2.2UF 20% 6.3V CERM 402-LF
OMIT C2241 2.2UF 20% 6.3V CERM 402-LF
OMIT C2242 2.2UF 20% 6.3V CERM 402-LF
OMIT C2243 2.2UF 20% 6.3V CERM 402-LF
OMIT C2213 10uF 20% 6.3V X5R 603
OMIT C2214 2.2UF 20% 6.3V CERM 402-LF
OMIT C2215 2.2UF 20% 6.3V CERM 402-LF
C2216 0.47UF 10% 6.3V CERM-X5R 402
C2217 0.1UF 10% 6.3V X5R 201
C2218 0.1UF 10% 6.3V X5R 201

PLACEMENT_NOTE=Place in GMCH cavity Place smaller caps as close as possible to NB pins.

NEED TO FIND A "1£GH, 500MA, 78MOHM" INDUCTOR
L2220 1.0UH-0.5A-0.675A 1007
=PP1V8_S0_NB_LVDS
260 mA
CRITICAL C2220 220UF 20% 2.5V POLY CASE-B2-SM-HF
C2221 1000PF 10% 16V X7R 201
PP1V8_S0_NB_VCCTXLVDS
MIN_LINE_WIDTH=0.2 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.8V
110 mA
C2223 1000PF 10% 16V X7R 201
Place C2221,C2223 close between J45,L45,J43 and K44
=GND_NB_VSSA_LVDS
Layout Note: Route to cap, then GND

=PP1V8_S0_NB_VCCD_LVDS
150 mA
C2226 22UF 20% 6.3V CERM 805
Place C2226 close to Pins J47, L47

CRITICAL C2298 22000pF-1000mA 16V NFM18
PP3V3_S0_NB_VCCA_DAC_BG
MIN_LINE_WIDTH=0.2 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=3.3V
5 mA
C2299 0.01UF 10% 10V X5R 201
C2297 0.1UF 10% 6.3V X5R 201
=GND_NB_VSSA_DAC_BG
Layout Note: Route to caps, then GND

GFX_VID<0>
GFX_VID<1>
GFX_VID<2>
GFX_VID<3>
=PP3V3_S0_NB_VCCHV
R2242 22K 5% 1/20W MF 201
R2243 22K 5% 1/20W MF 201
R2244 22K 5% 1/20W MF 201
R2245 22K 5% 1/20W MF 201
R2247 22K 5% 1/20W MF 201
R2248 22K 5% 1/20W MF 201
R2249 22K 5% 1/20W MF 201
NO STUFF R2250 22K 5% 1/20W MF 201

=PP3V3_S0_NB_VCCSYNC
10 mA
C2230 0.1UF 10% 6.3V X5R 201
Place C2230 close to Pin L35

CRITICAL U2265 TPS731125 SOT23-5
Vout = 1.204V * (Ra + Rb)/Rb
Ra || Rb should be 19Kohms
WARNING VOLTAGE DROP
=PP1V8_S0_NB_DPLL
(1.7V - 5.5V)
80 mA
OMIT C2265 1UF 10% 6.3V CERM 402
IN EN OUT NR/FB GND
PP1V25_S0_NB_DPLL
MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.25V
P1V25S0NBDPLL_FB
OMIT C2266 10UF 20% 6.3V X5R 603
P1V25S0NBDPLL_RF
C2267 0.01UF 10% 10V X5R 201
R2266 0.300 5% 1/10W FF 603

80 mA
R2261 0 5% 1/10W MF-LF 402
PP1V25_S0_NB_VCCA_DPLLA
MIN_LINE_WIDTH=0.3 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.25V
C2261 0.1UF 10% 6.3V X5R 201
Place C2261 close to Pin D50
R2262 0 5% 1/10W MF-LF 402
OMIT C2260 10uF 20% 6.3V X5R 603
PP1V25_S0_NB_VCCA_DPLLB
MIN_LINE_WIDTH=0.3 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.25V
C2262 0.1UF 10% 6.3V X5R 201
Place C2262 close to Pin J49
80 mA

Current numbers from Crestline EDS Addendum, doc #20127.

NB Graphics Decoupling

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 22 OF 109	

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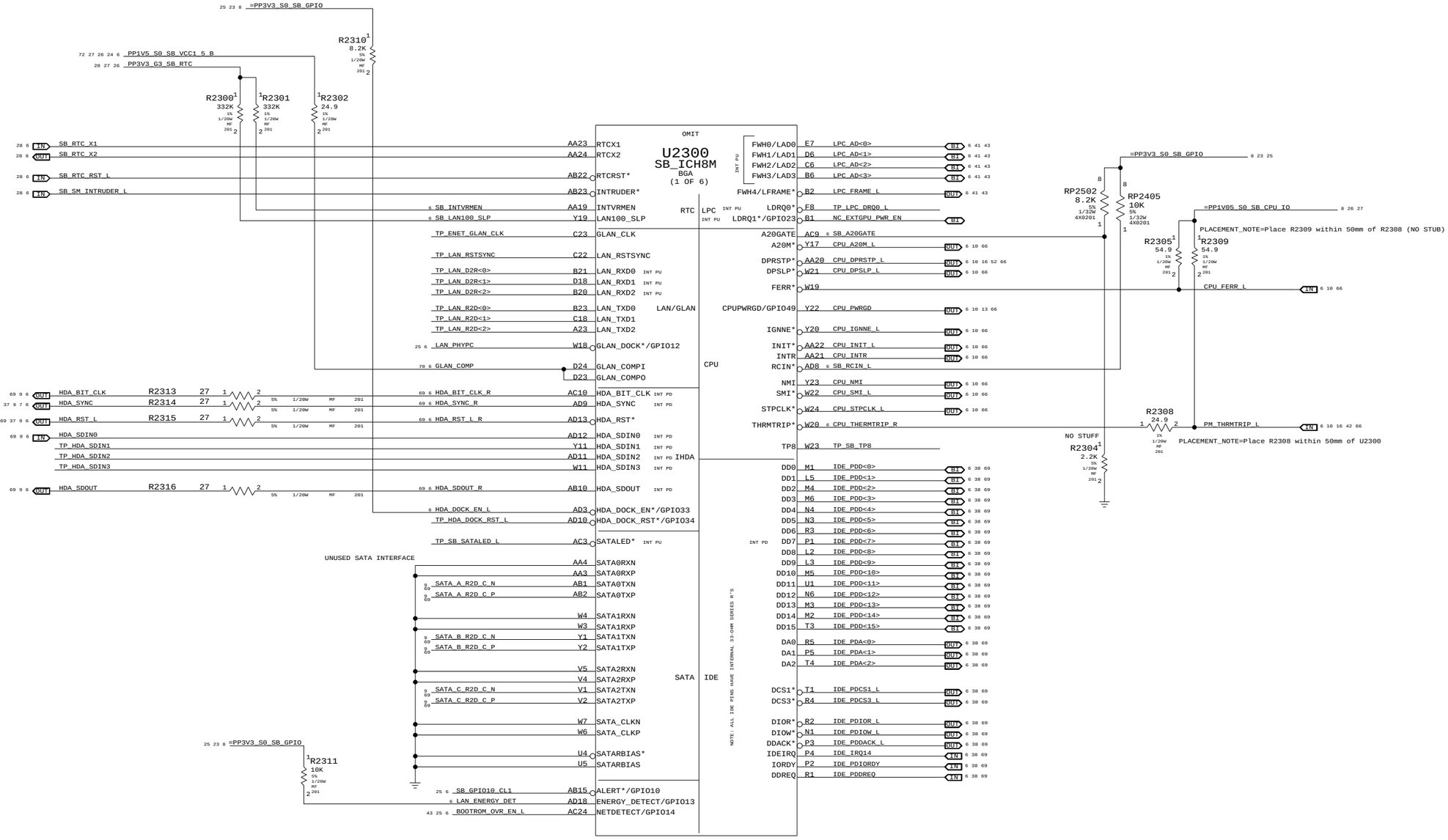

	HDA
HDA_BIT_CLK	24.000MHZ CLOCK W/INTERNAL WEAK PD
HDA_RST#	
HDA_SDIN[0-2]	INTEGRATED PDs
HDA_SDOUT	INTEGRATED PD
ACZ_SYNC	INTEGRATED PD

SB Enet, Disk, FSB, LPC

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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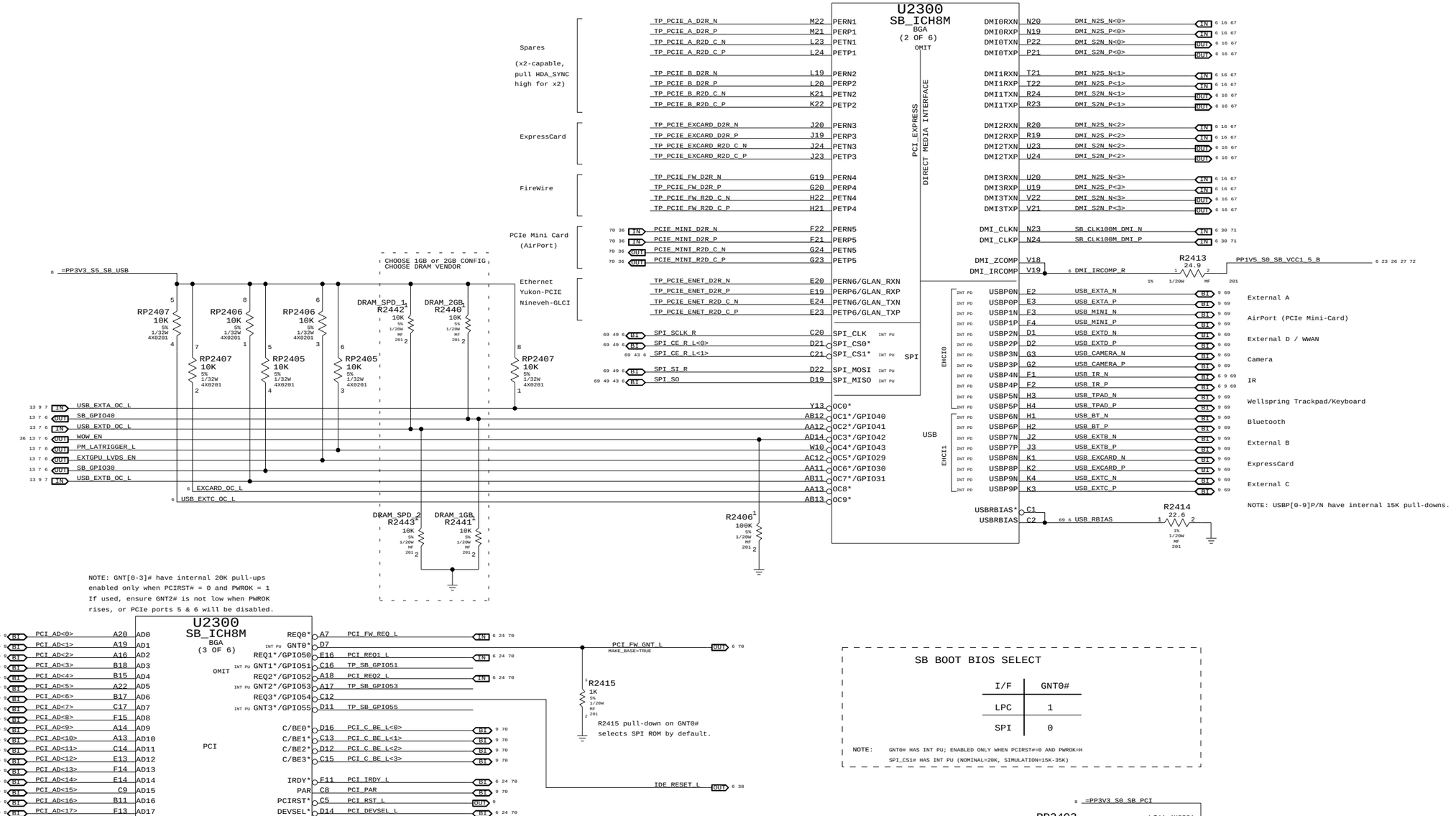
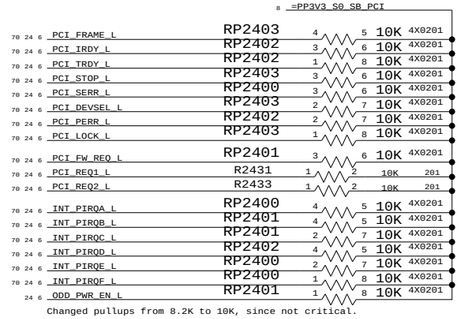


SB BOOT BIOS SELECT

I/F	GNT0#
LPC	1
SPI	0

NOTE: GNT0# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
SPI_CS1# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)



Changed pullups from 8.2K to 10K, since not critical.

SB PCI, PCIe, DMI, USB

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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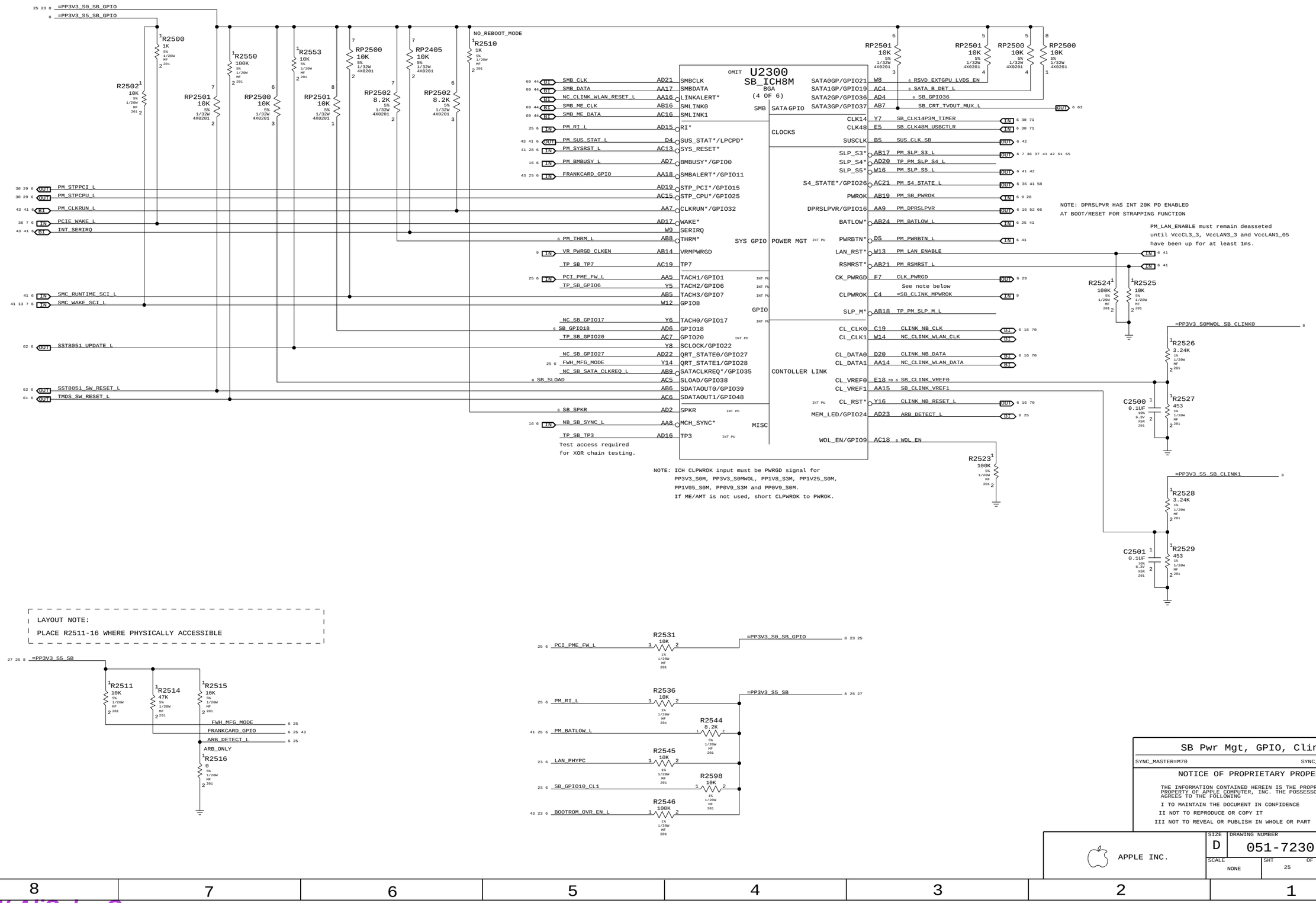

SB Pwr Mgt, GPIO, Clink

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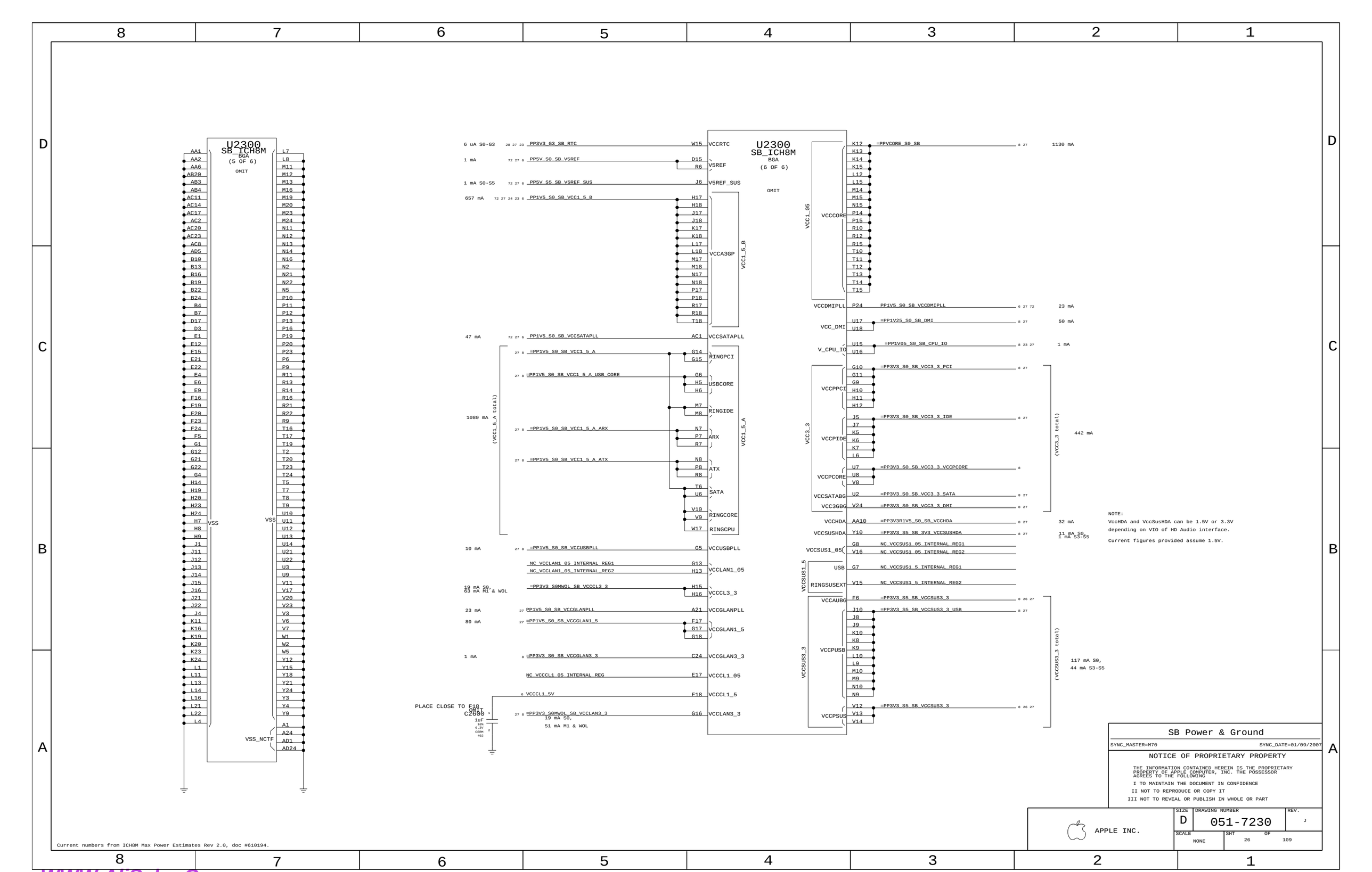

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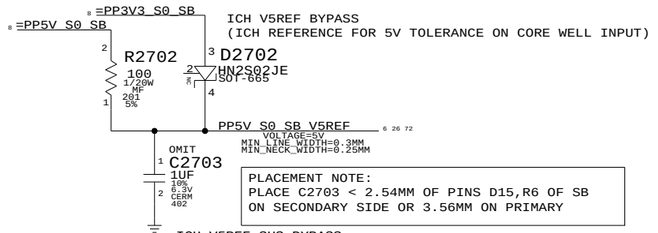
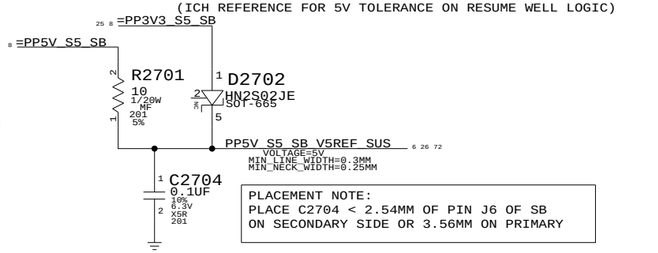
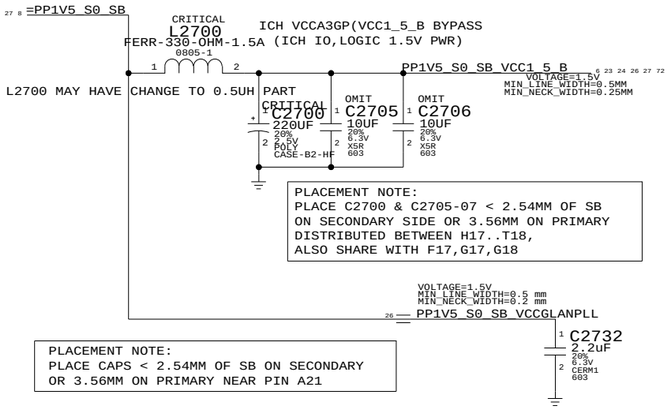
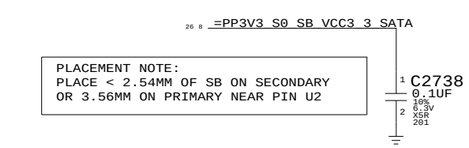
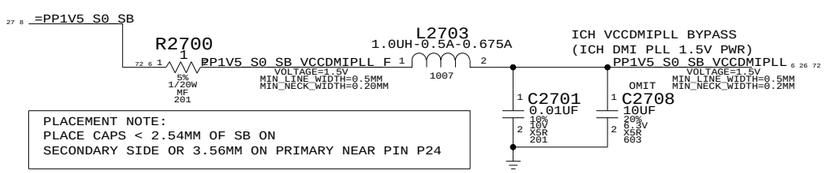
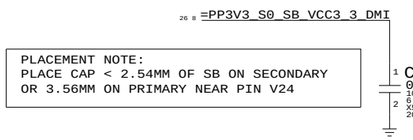


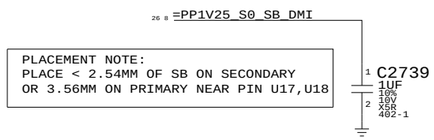


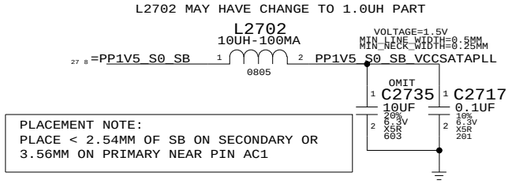


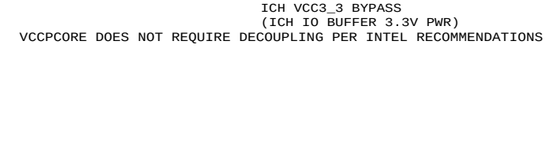


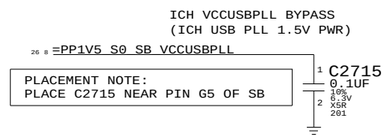


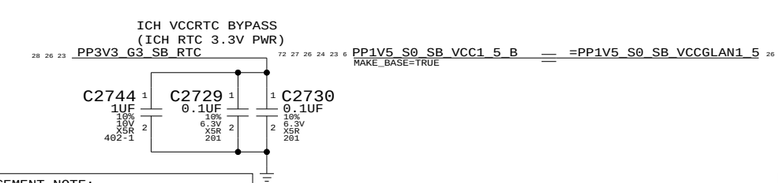


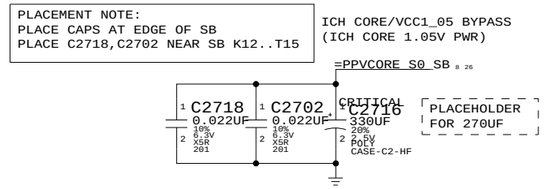


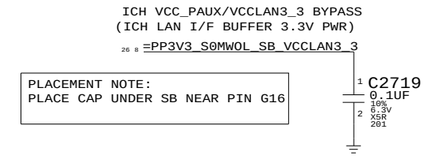


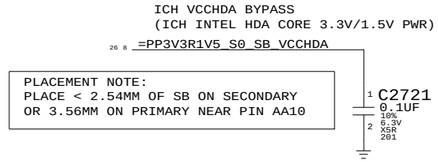


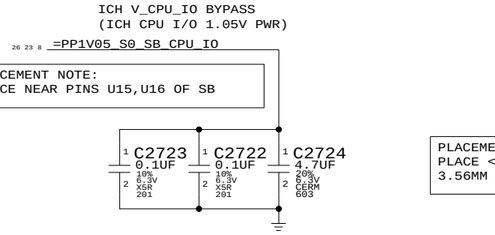


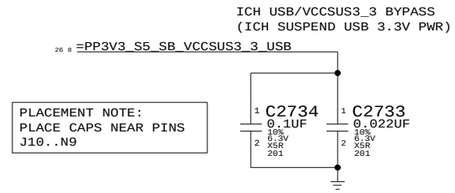


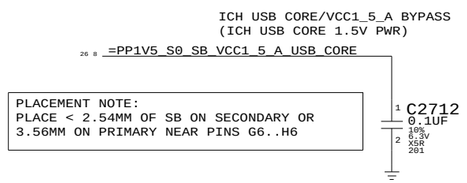


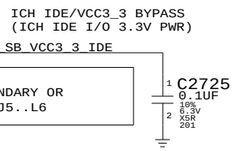




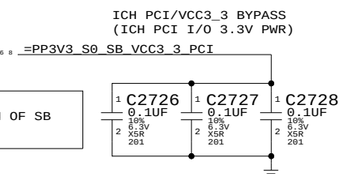


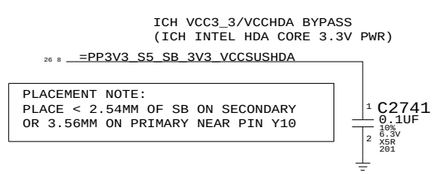






VCCCL3_3 DOES NOT REQUIRE DECOUPLING PER INTEL RECOMMENDATIONS





SB Decoupling

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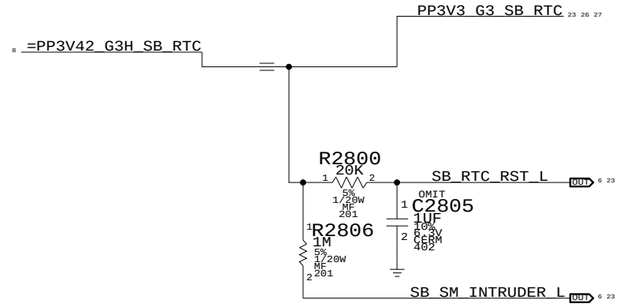
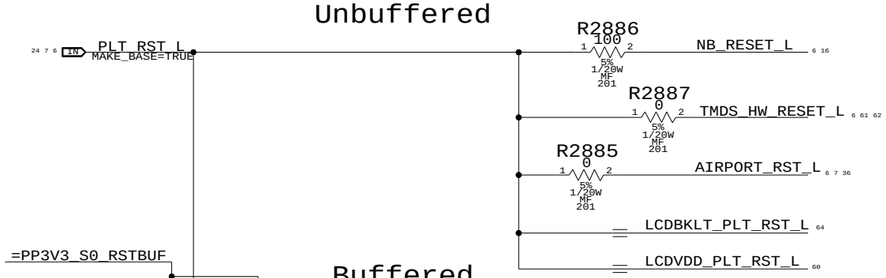
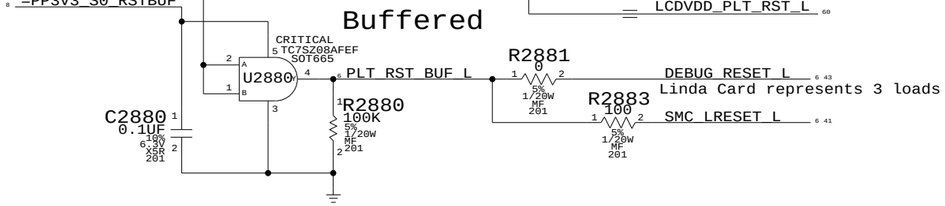


Platform Reset Connections

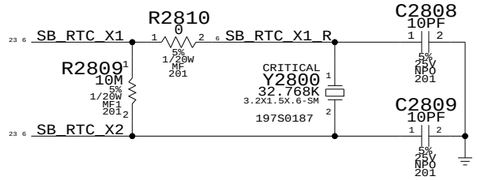
Unbuffered

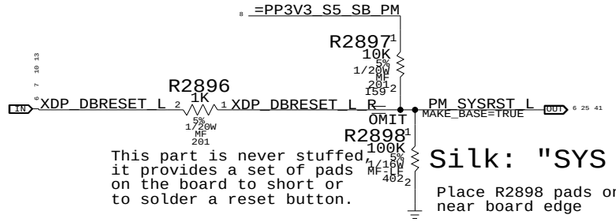


Buffered



SB RTC Crystal Circuit

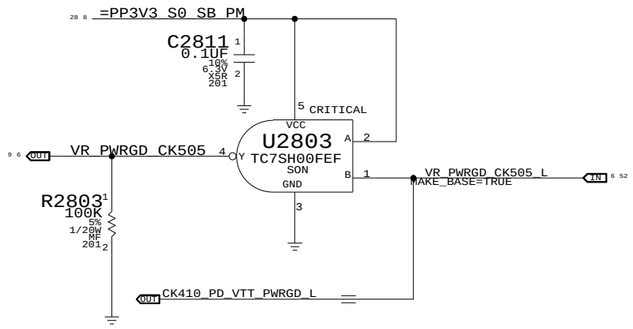


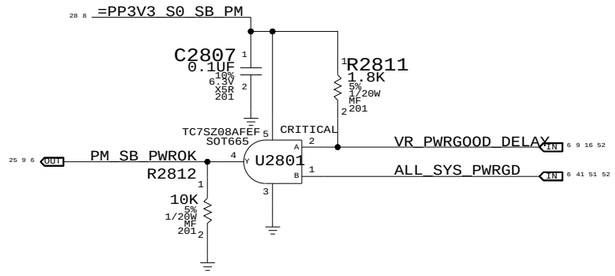


This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

Silk: "SYS RST"

Place R2898 pads on bottom side near board edge





SB Misc

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SCALE	SHT	OF
NONE	28	109

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Silego recommend to remove L2903,R2900,C2907,C2910
R2901,L2902,C2916,C2911,C2914 and R2902

=PP3V3_S0_CK505

CRITICAL
L2901
FERR-120-OHM-1.5A
0402-LF
MIN_LINE_WIDTH=0.5mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=3.3V

PP3V3_S0_CK505_VDD_CPU_SRC

OMIT C2900 1UF 10% 6.3V CERM 402

OMIT C2901 10UF 20% 6.3V X5R 603

C2902 0.1UF 10% 6.3V X5R 201
C2903 0.1UF 10% 6.3V X5R 201
C2904 0.1UF 10% 6.3V X5R 201
C2905 0.1UF 10% 6.3V X5R 201
C2906 0.1UF 10% 6.3V X5R 201
C2908 0.1UF 10% 6.3V X5R 201
C2909 0.1UF 10% 6.3V X5R 201
C2912 0.1UF 10% 6.3V X5R 201
C2913 0.1UF 10% 6.3V X5R 201
C2915 0.1UF 10% 6.3V X5R 201

CRITICAL
Y2901
SM-2.5X2.0MM
14.318MHZ-35PPF-20PF
C2989 20PF 5% 25V NP0-C0G 201
C2990 20PF 5% 25V NP0-C0G 201

(EACH POWER PIN PLACED ONE 0.1UF)
(PLACED 0.1UF NEAR THE RELATIVE POWER PIN)

U2900
SLG2AP101
QFN

3	VDD_48		
43	VDD_CPU		
61	VDD_PCI		
67			
49	VDD_REF		
12	VDD_SRC		
17			
28			
35			
38	VDD_A		
39	VSS_A		
51	XTAL_IN	CK505_XTAL_IN	
50	XTAL_OUT	CK505_XTAL_OUT	6
8	FS_B/TEST_MODE	CK505_FSB_TEST_MODE	30 6 IN
57	PCI_1	TP_CK505_PCI1_CLK	9 OUT
58	PCI_2	TP_CK505_PCI2_CLK	9 OUT
63	PCI_3	CK505_PCI3_CLK	71 30 6 OUT
64	PCI_4	TP_CK505_PCI4_CLK	9 OUT
65	PCI_5/FCT_SEL	CK505_PCI5_FCTSEL1	BI
68	PCIF_0/ITP_EN	CK505_PCIF0_CLK	30 6 OUT
1	PCIF_1	CK505_PCIF1_CLK	30 6 71 OUT
47	SCL	=SMBUS_CK505_SCL	44 IN
48	SDA	=SMBUS_CK505_SDA	44 BI
5	VSS_48		
46	VSS_CPU		
62			
66	VSS_PCI		
52	VSS_REF		
31	VSS_SRC		
69	THRM_PAD		
56	PCI_STOP*	PM_STPPCI_L	6 25 30 IN
55	CPU_STOP*	PM_STPCPU_L	6 25 30 IN
44	CPU_0*	CK505_CPU0_N	30 71 OUT
45	CPU_0	CK505_CPU0_P	30 71 OUT
41	CPU_1_MCH*	CK505_CPU1_N	30 71 OUT
42	CPU_1_MCH	CK505_CPU1_P	30 71 OUT
36	CPU_ITP*/SRC_10*	CK505_CPU2_ITP_SRC10_N	30 71 OUT
37	CPU_ITP/SRC_10	CK505_CPU2_ITP_SRC10_P	30 71 OUT
11	SRC_0*/LCD_CLK*	CK505_LVDS_N	30 71 OUT
10	SRC_0/LCD_CLK	CK505_LVDS_P	30 71 OUT
14	SRC_1*	TP_CK505_SRC1_N	9 OUT
13	SRC_1	TP_CK505_SRC1_P	9 OUT
9	CLKREQ_1* (INT PU)	TP_CK505_SRC_CLKREQ1_L	9 IN
16	SRC_2*	CK505_SRC2_N	30 71 OUT
15	SRC_2	CK505_SRC2_P	30 71 OUT
19	SRC_3*	TP_CK505_SRC3_N	9 OUT
18	SRC_3	TP_CK505_SRC3_P	9 OUT
59	CLKREQ_3* (INT PU)	TP_CK505_SRC_CLKREQ3_L	9 IN
22	SRC_4*	TP_CK505_SRC4_N	9 OUT
21	SRC_4	TP_CK505_SRC4_P	9 OUT
20	CLKREQ_4* (INT PU)	TP_CK505_SRC_CLKREQ4_L	9 IN
24	SRC_5*	CK505_SRC5_N	30 71 OUT
23	SRC_5	CK505_SRC5_P	30 71 OUT
60	CLKREQ_5* (INT PU)	NB_CLKREQ_L	6 16 IN
27	SRC_6*	CK505_SRC6_N	30 71 OUT
26	SRC_6	CK505_SRC6_P	30 71 OUT
25	CLKREQ_6* (INT PU)	CK505_SRC_CLKREQ6_L	6 7 36 IN
30	SRC_7*	TP_CK505_SRC7_N	9 OUT
29	SRC_7	TP_CK505_SRC7_P	9 OUT
40	CLKREQ_7* (INT PU)	TP_CK505_PGMODE	9
32	SRC_8*	TP_CK505_SRC8_N	9 OUT
33	SRC_8	TP_CK505_SRC8_P	9 OUT
34	CLKREQ_8* (INT PU)	TP_CK505_SRC_CLKREQ8_L	9 IN
7	DOT_96*/27M_SS	CK505_DOT96_27M_N	30 71 OUT
6	DOT_96/27M (INT PD)	CK505_DOT96_27M_P	30 71 OUT
2	CKPWRGD/PD*	CLK_PWRGD	6 25 IN
4	48M/FS_A	CK505_USB48_FSA	6 30 OUT
54	REF_0/FS_C/TEST_SEL	CK505_CLK14P3M_TIMER	6 30 OUT
53	GPU_STOP*	TP_GPU_STOP_L	9 BI

(FROM ICH8M GPIO15 STPPCI*)
(FROM ICH8M GPIO25 STPCPU*)
(CPU HOST 133/167MHZ)
(GMCH HOST 133/167MHZ)
(ITP HOST 133/167MHZ)
(GMCH D_REFSSCLKIN DISPLAY PLL B 100MHZ)
(SLOT F - GPU PCI-E 100 MHZ)
(ICH8M DMI 100 MHZ)
(SLOT D - 4 LANE PCI-E FOR EXPRESSCARD)
(ICH SATA 100 MHZ)
(FROM ICH8M GPIO35)
(GMCH G_CLKIN 100 MHZ)
(FROM GMCH CLK_REQ*)
(WIRELESS PCI-E 100 MHZ)
(DB400 SRC)
(SLOT E)
(GMCH D_REFCLKIN DISPLAY PLL A 96MHZ)
(FROM ICH8M)
(ICH8M USB 48MHZ)
(ICH8M,SIO,LPC REF. 14.318MHZ)

=PP3V3_S0_CK505

R2903 10K 5% 1/20W MF 201

(FW PCI 33MHZ)
(TPM LPC 33MHZ)
(SMC LPC 33MHZ)
(PCI SLOT)
(PORT80 LPC 33MHZ)
(ICH8M PCI 33MHZ)
(PULL UP PIN 68 TO ENABLE ITP HOST CLK)
(ICH SM BUS)

(NO INT PD)
(INT PU)
(NO INT PU)

FCTSEL1	PIN 6	PIN 7	PIN 10	PIN 11
0	DOT96T	DOT96C	100MT_SST	100MC_SST
1	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0

* FOR INT. GRAPHIC SYSTEM
* FOR EXT. GRAPHIC SYSTEM

Clock (CK505)

SYNC_MASTER=M70 SYNC_DATE=02/01/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7230	J

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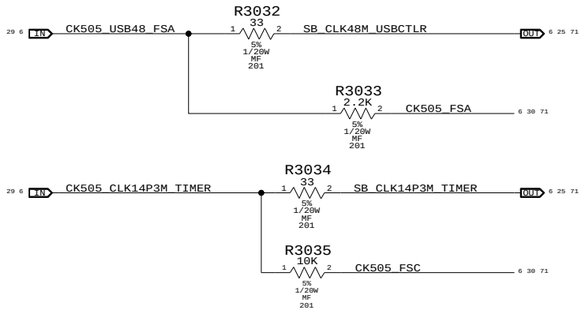
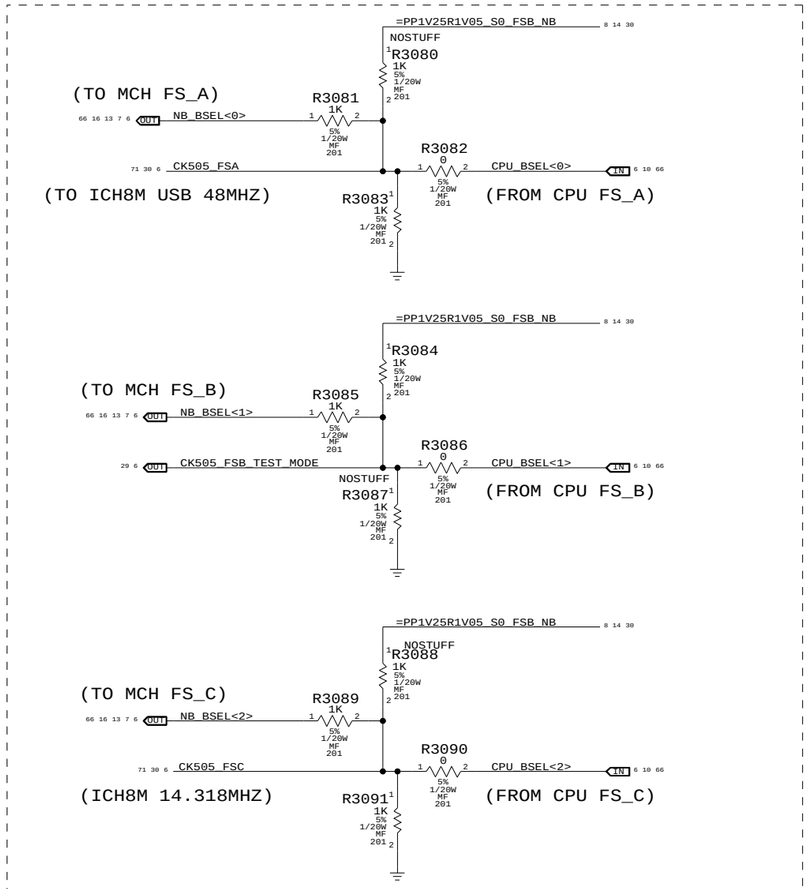
CLK Termination

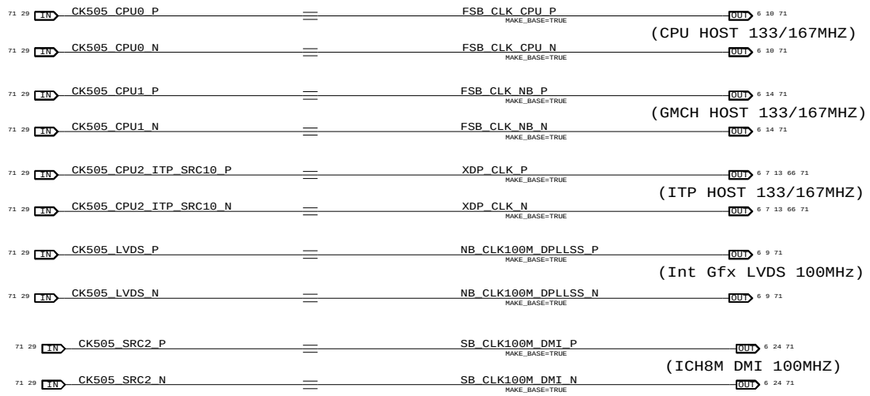


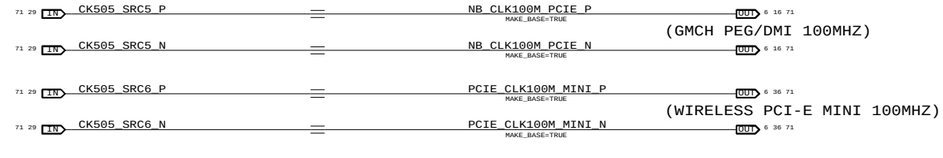


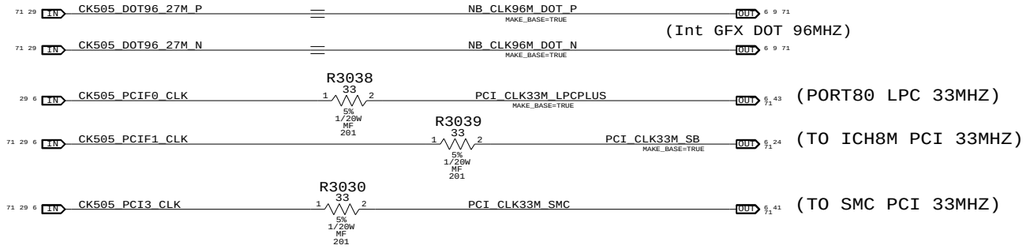
	FS_C	FS_B	FS_A	CPU
	0	0	0	266M
	0	0	1	133M
	0	1	1	166M
*	0	1	0	200M
	1	1	0	400M
	1	1	1	Resrvd
	1	0	1	100M
	1	0	0	333M

NOSTUFF R3082, R3086, R3090
FOR MANUAL CPU FREQUENCY

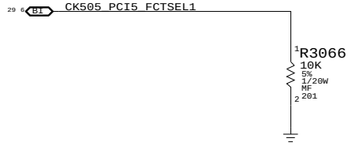
CPU speed is currently set to 200MHz







CLKREQ Controls



Clock Termination

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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SIZE	DRAWING NUMBER	REV.
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NONE	30	109

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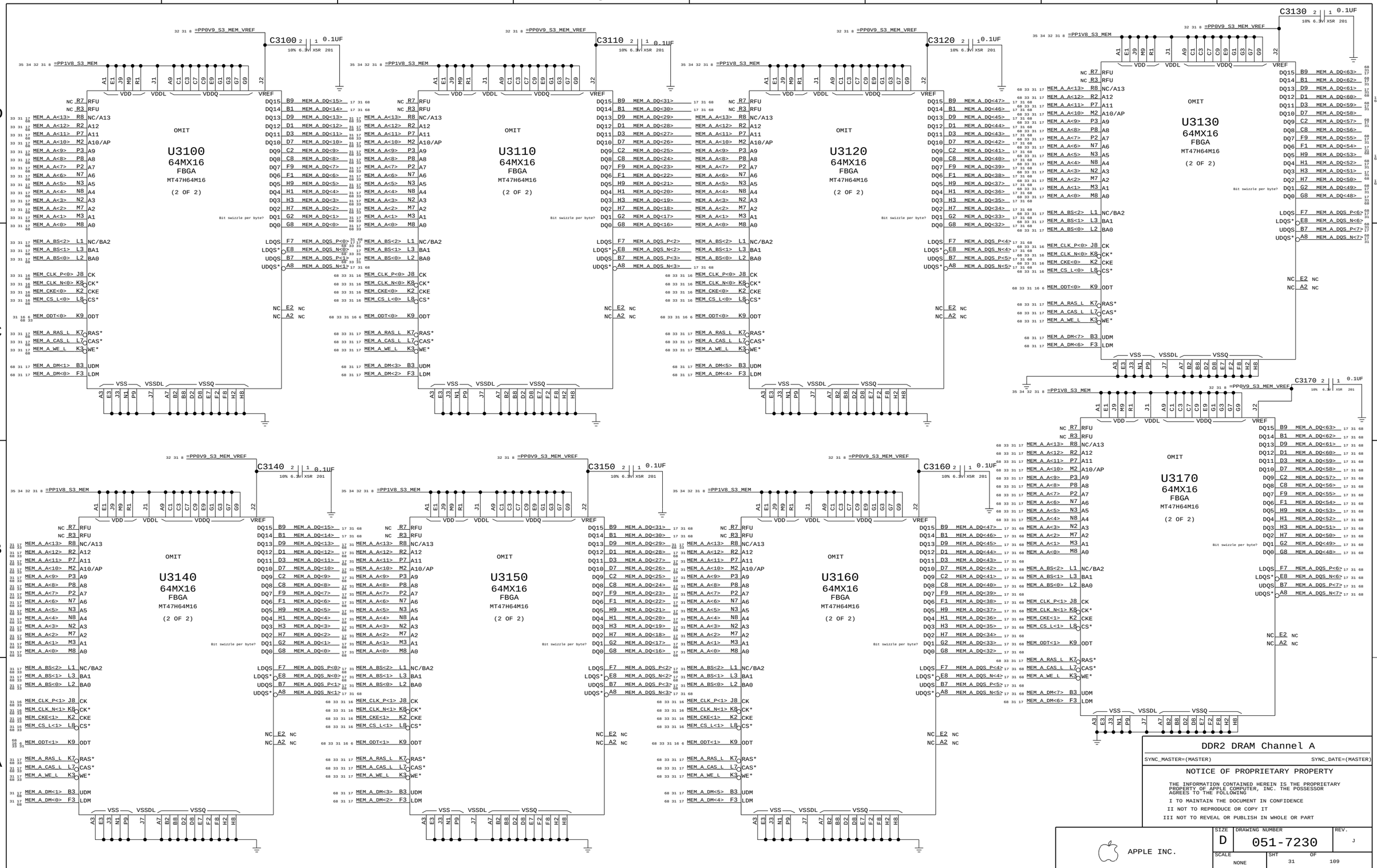

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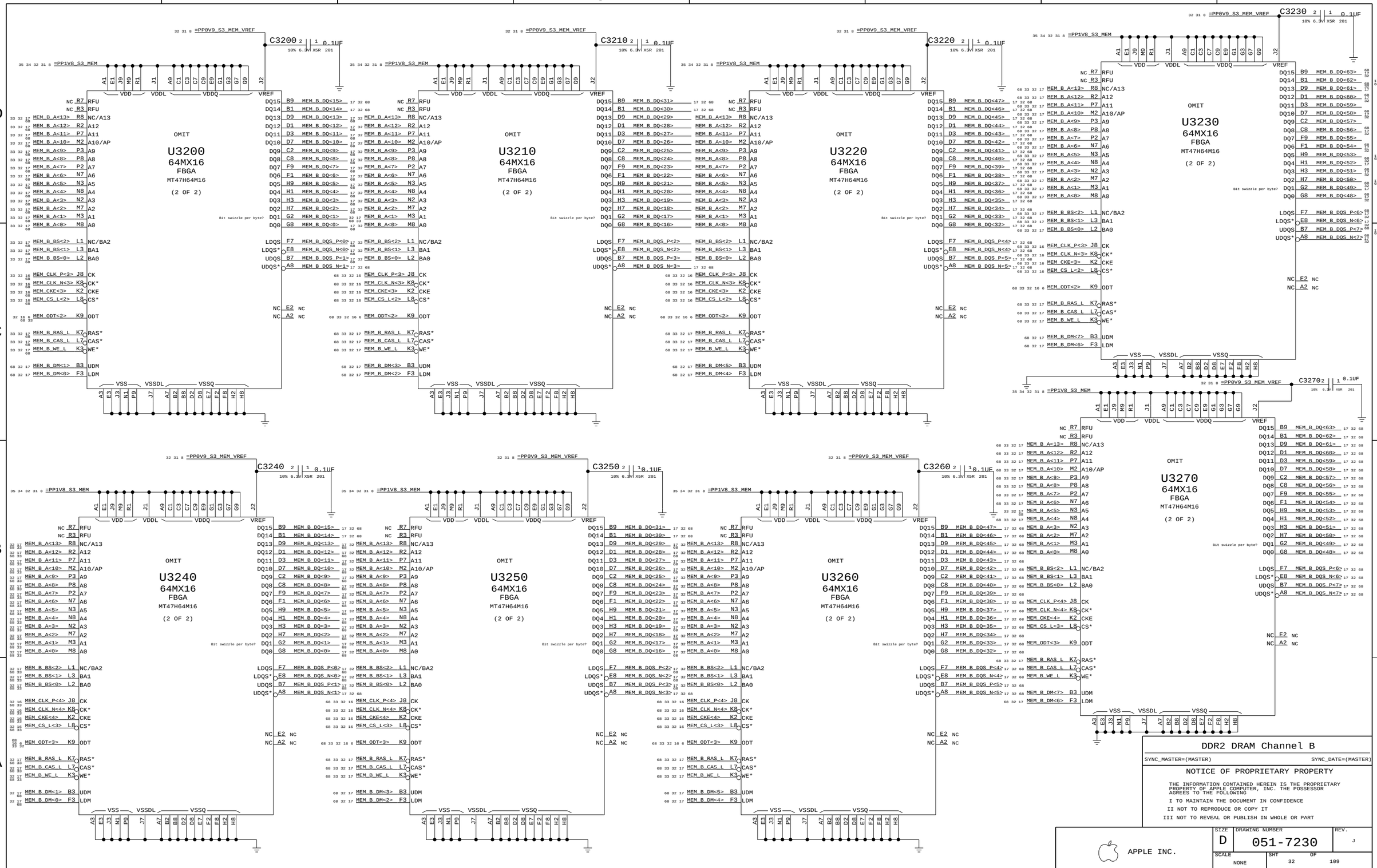

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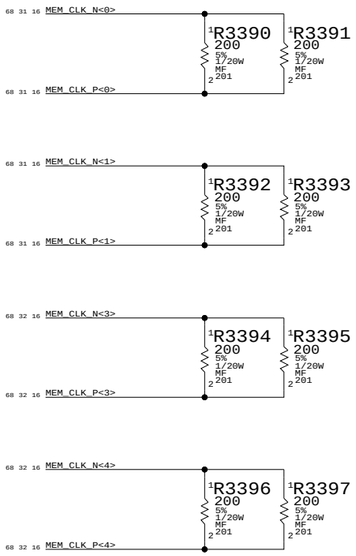
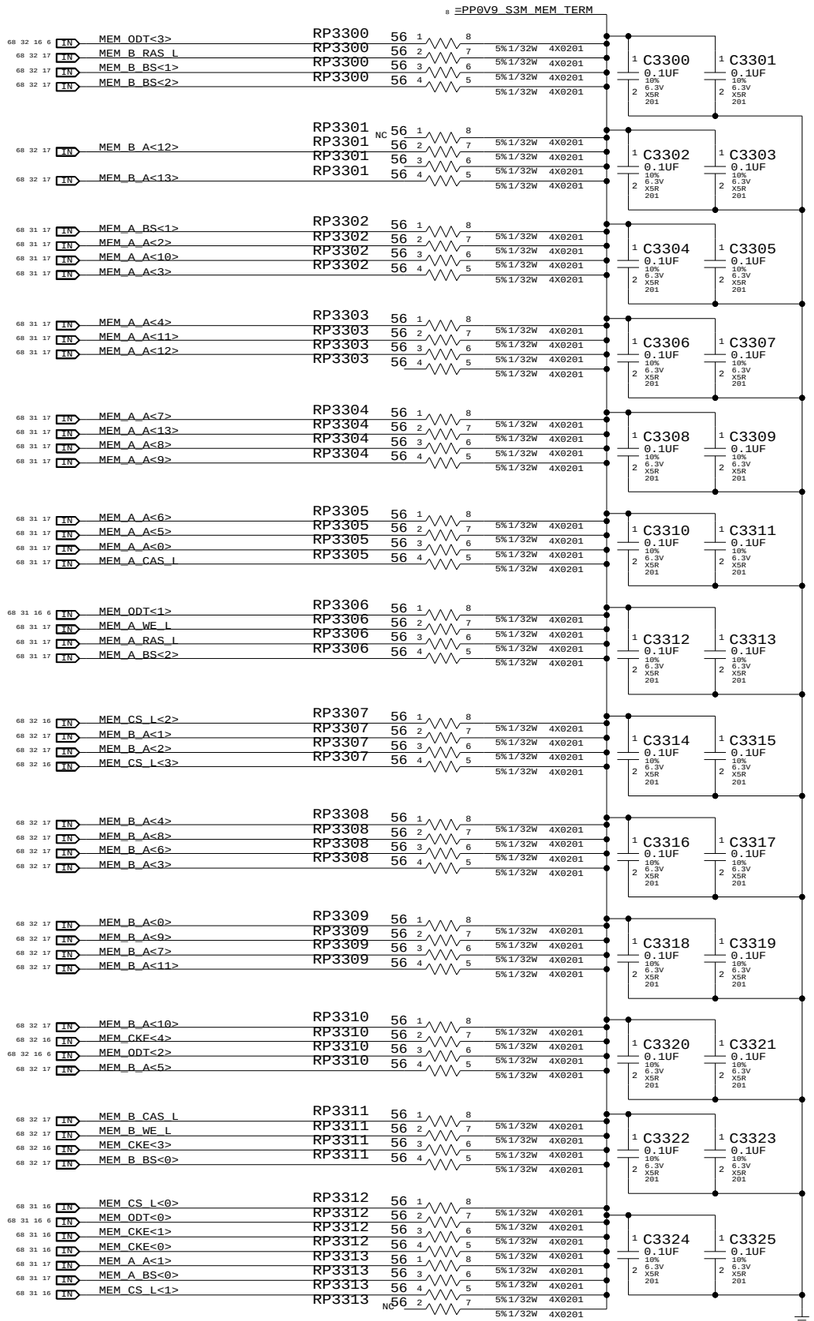
MEM CLOCK TERMINATION

Place one resistor at each end of Y split



One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



LAYOUT NOTE:PLACE ONE CAP CLOSE TO EVERY TWO PULLUP RESISTORS TERMINATED TO PP0V9_S0_MEM_TERM

Memory Active Termination

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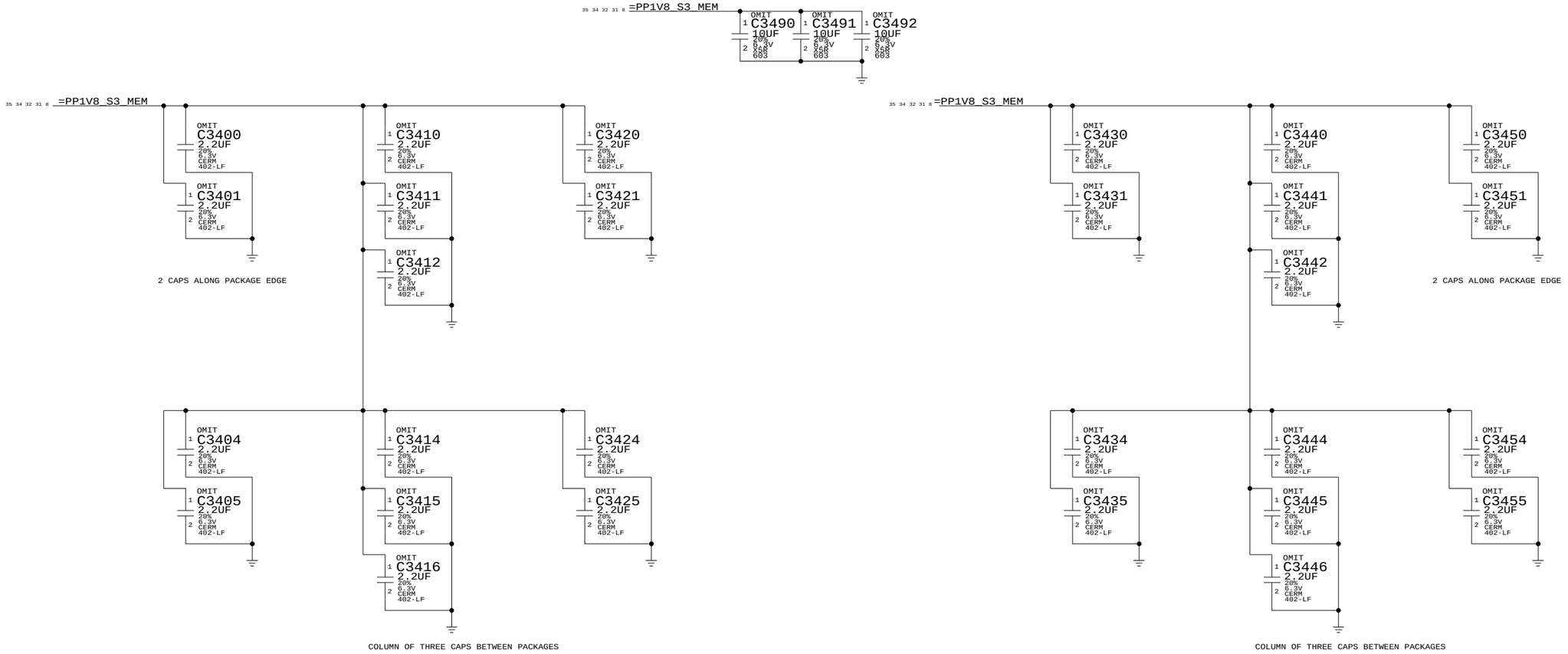
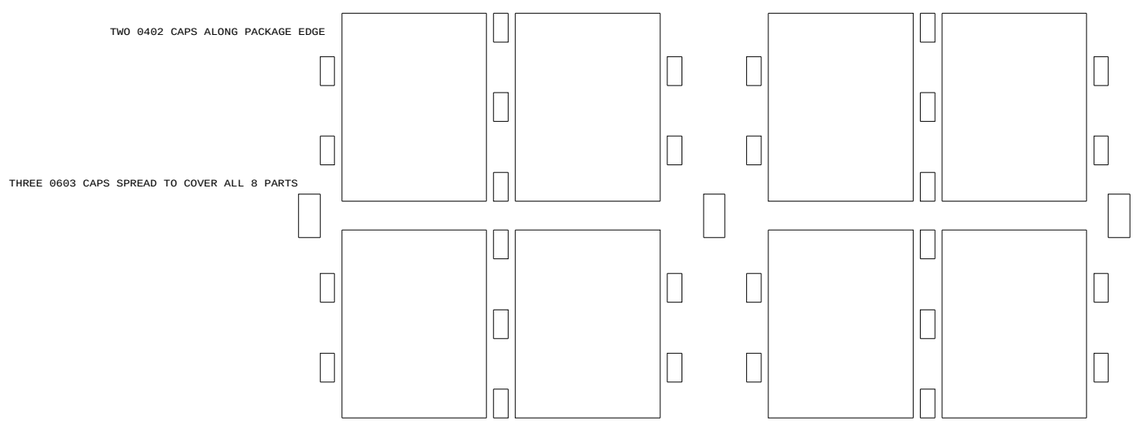


APPROXIMATE CAP ARRANGEMENT



COLUMN OF THREE 0402 CAPS BETWEEN PACKAGES

DDR2 BYPASSING 1

SYNC_MASTER=MEMORY SYNC_DATE=06/20/2005

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D	051-7230	J
SCALE: NONE	SHT 34 OF 109	

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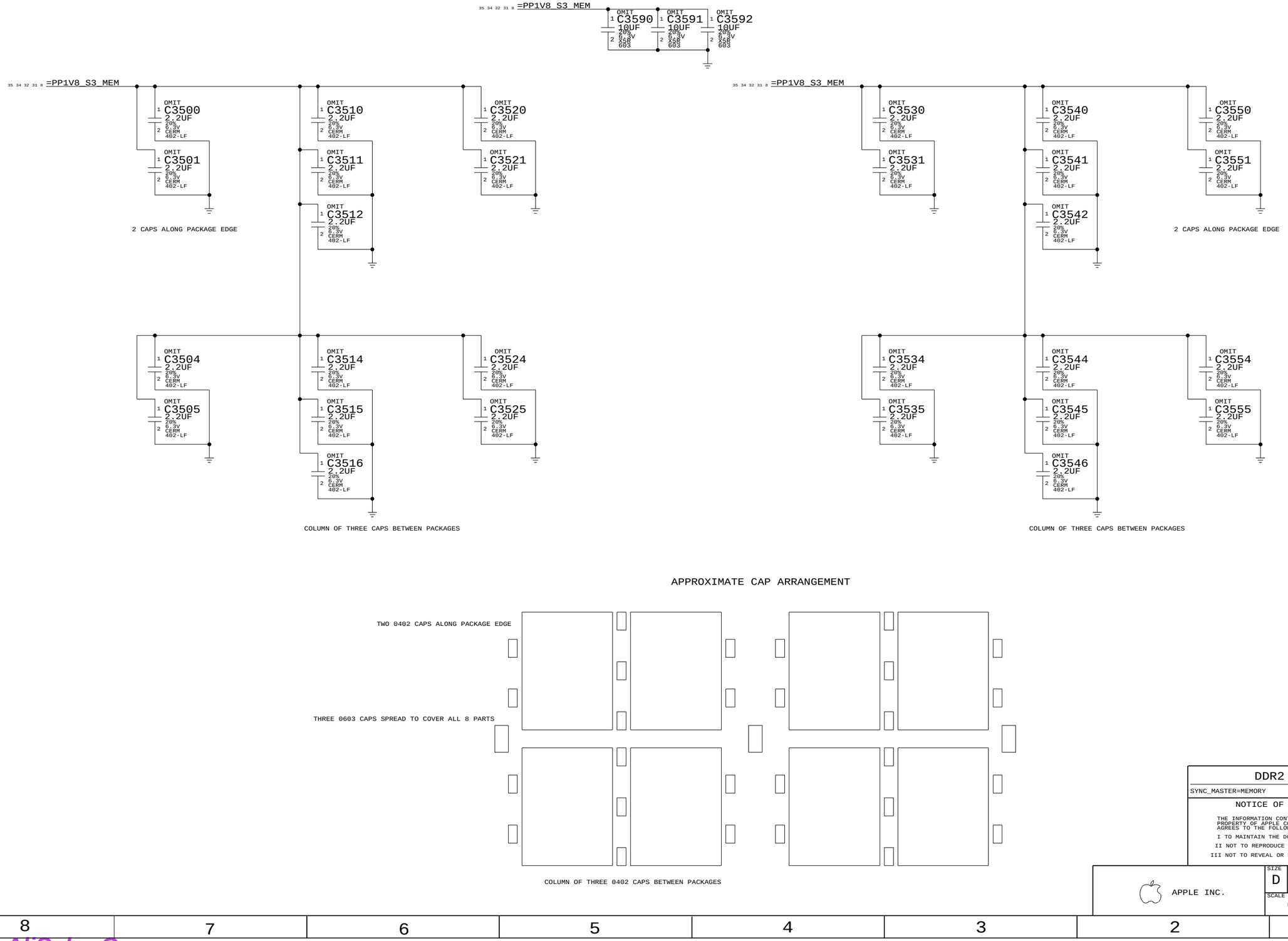

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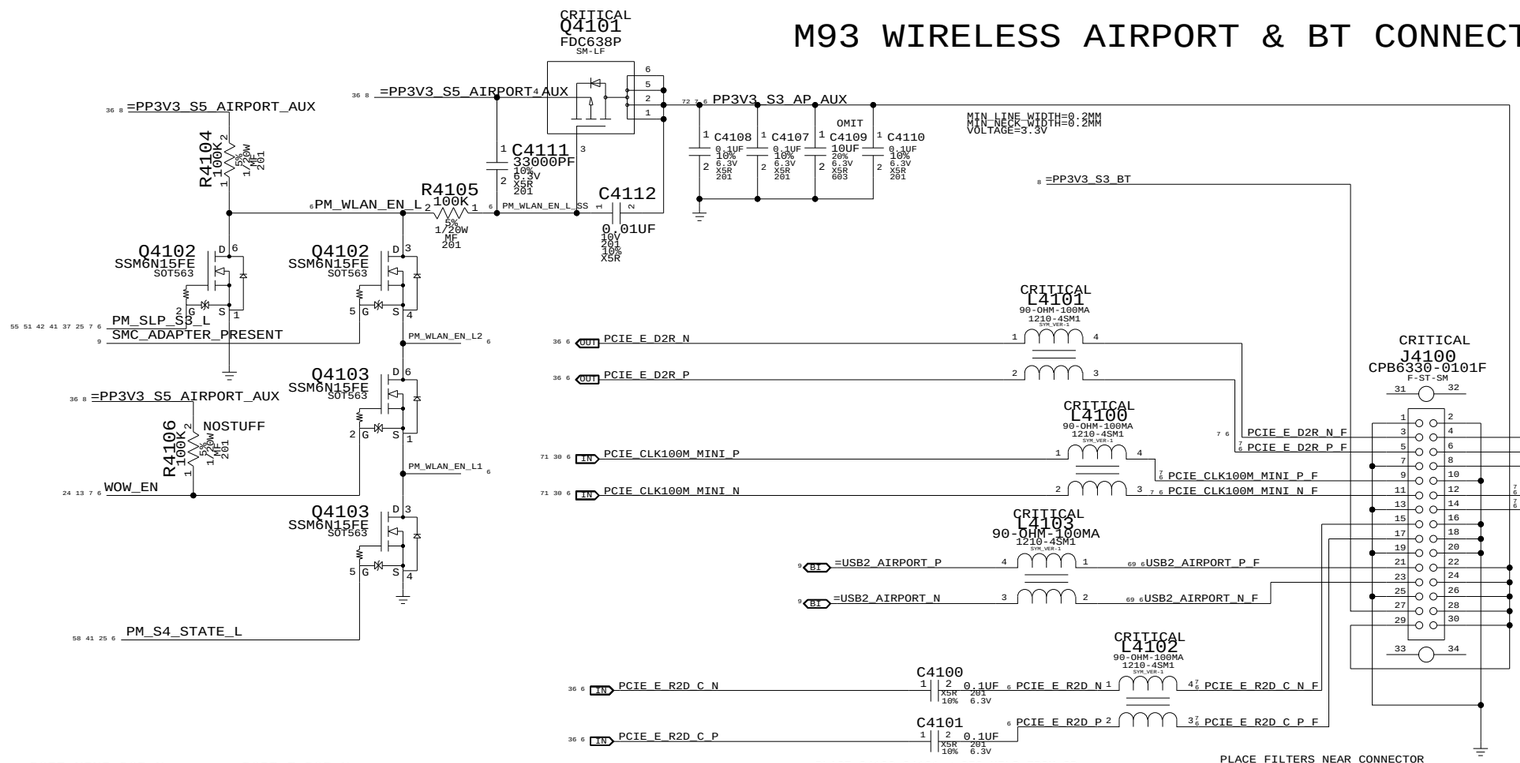
M93 WIRELESS AIRPORT & BT CONNECTOR



PCIE_MINI_D2R_N — PCIE_E_D2R_N — MAKE_BASE=TRUE
PCIE_MINI_D2R_P — PCIE_E_D2R_P — MAKE_BASE=TRUE
PCIE_MINI_R2D_C_N — PCIE_E_R2D_C_N — MAKE_BASE=TRUE
PCIE_MINI_R2D_C_P — PCIE_E_R2D_C_P — MAKE_BASE=TRUE

APN:516S0580

Wireless M93 Connector

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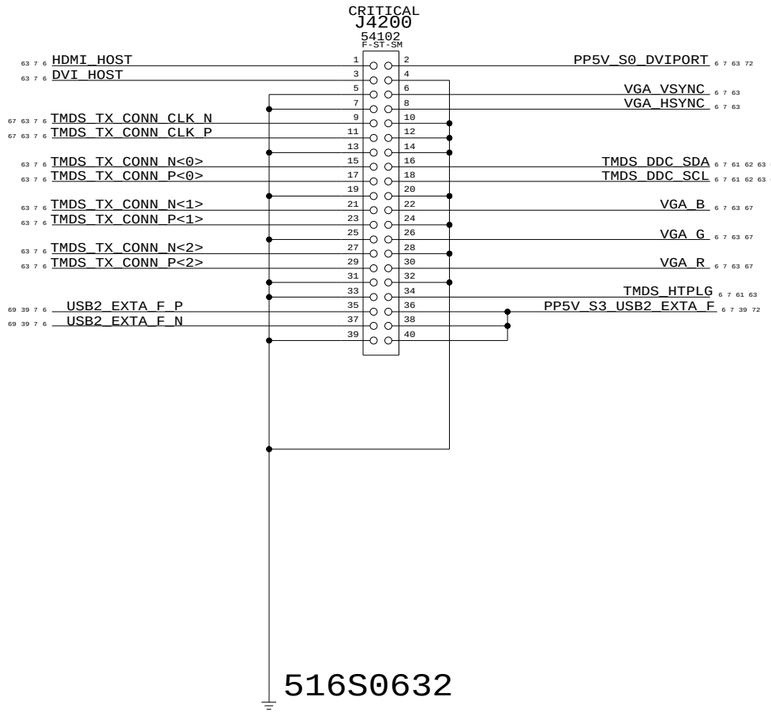
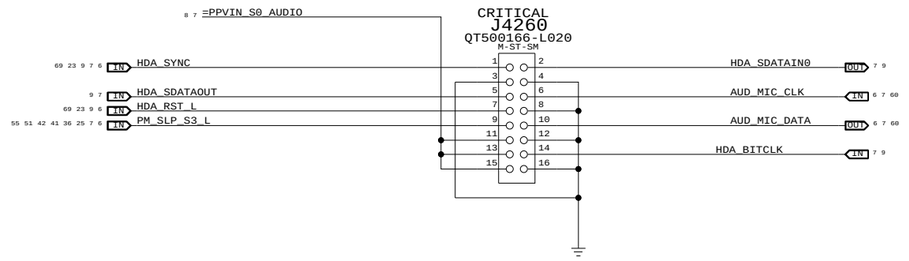
Micro DVI, USB, to RIO Hatch Assembly



516S0632

Audio Connector



516S0350

Hatch and Audio Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE	SHT OF	
NONE	42 109	

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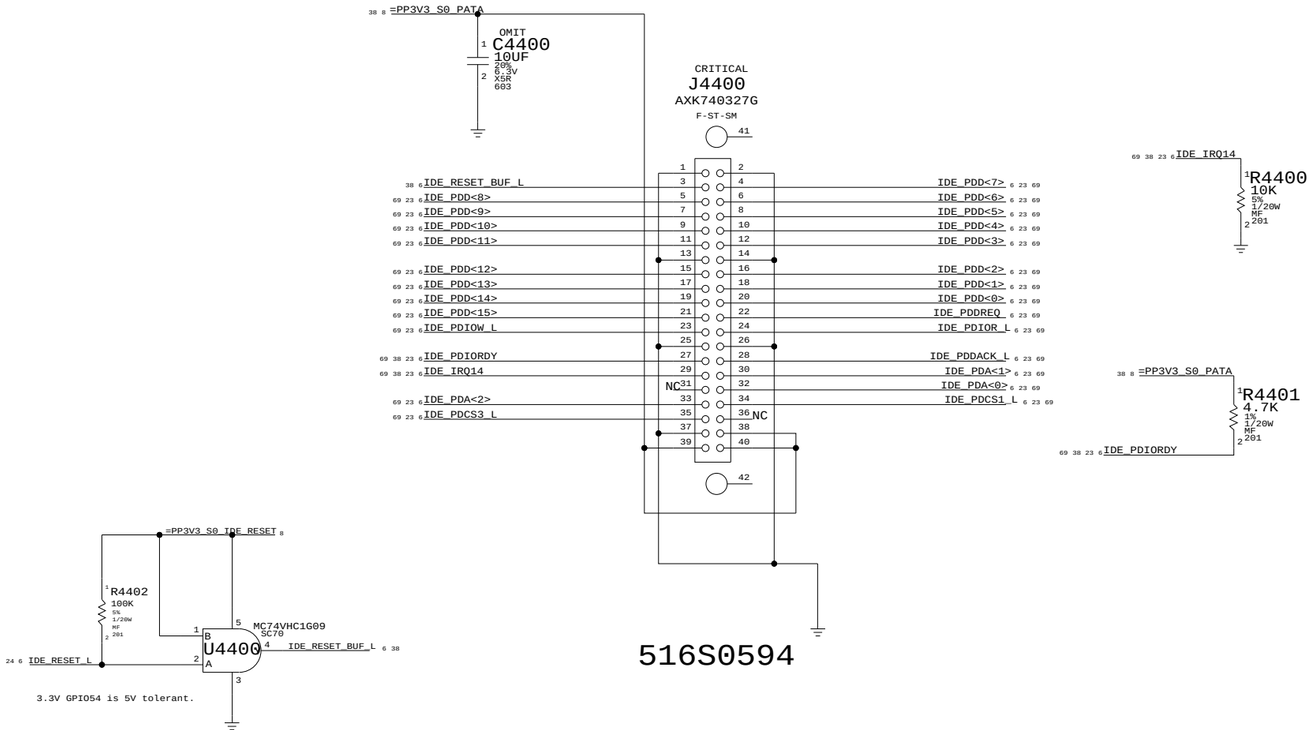

PATA HDD CONNECTOR

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SCALE	SHT	OF
NONE	44	109

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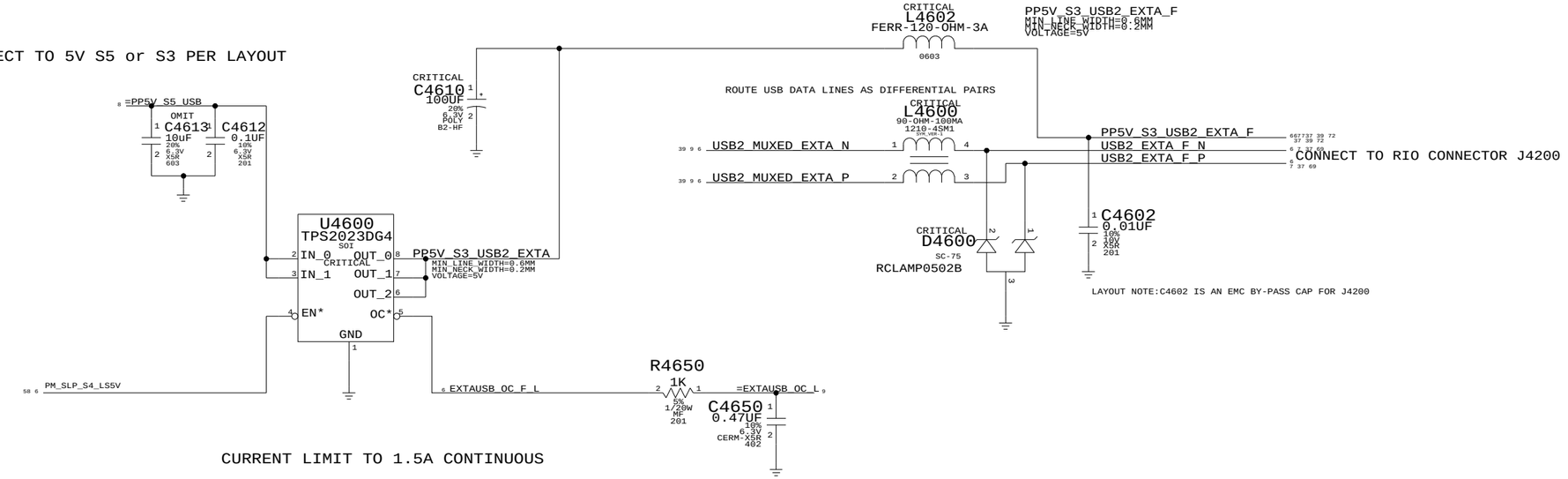
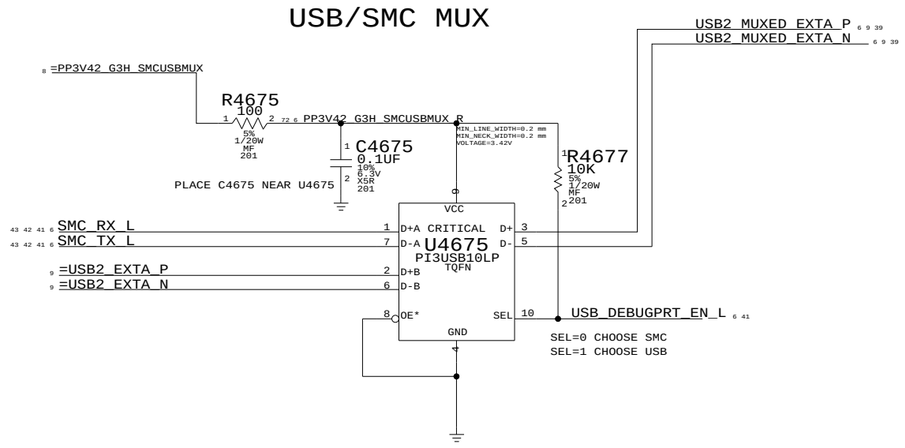
USB 2.0 CONNECTOR

CONNECT TO 5V S5 or S3 PER LAYOUT



CURRENT LIMIT TO 1.5A CONTINUOUS

USB/SMC MUX



USB EXTERNAL CONNECTORS

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 46 OF 109	

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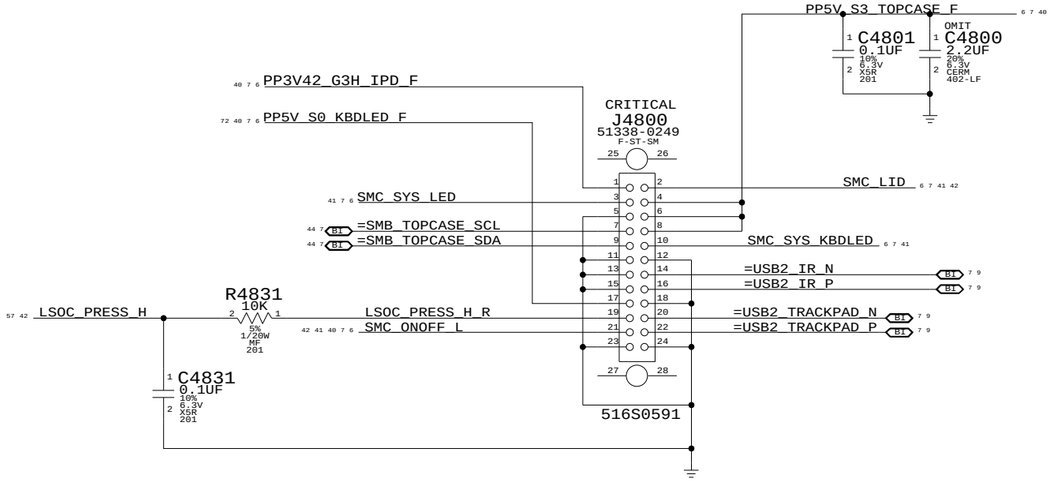
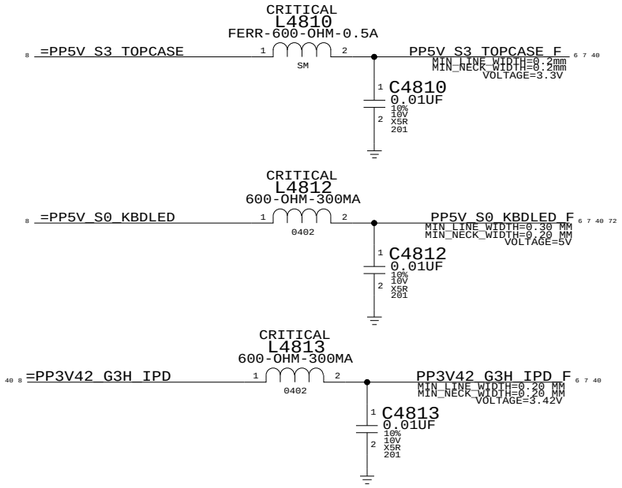
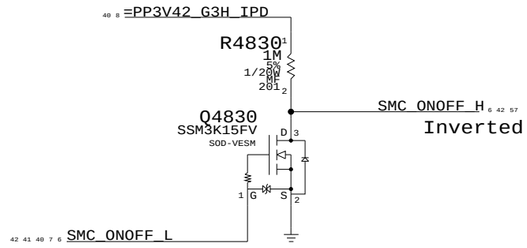
IPD Connector





Power Button Inverter



Inverted to drive SMC_RESET logic

IPD Connector

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SCALE	SHT	OF
NONE	48	109

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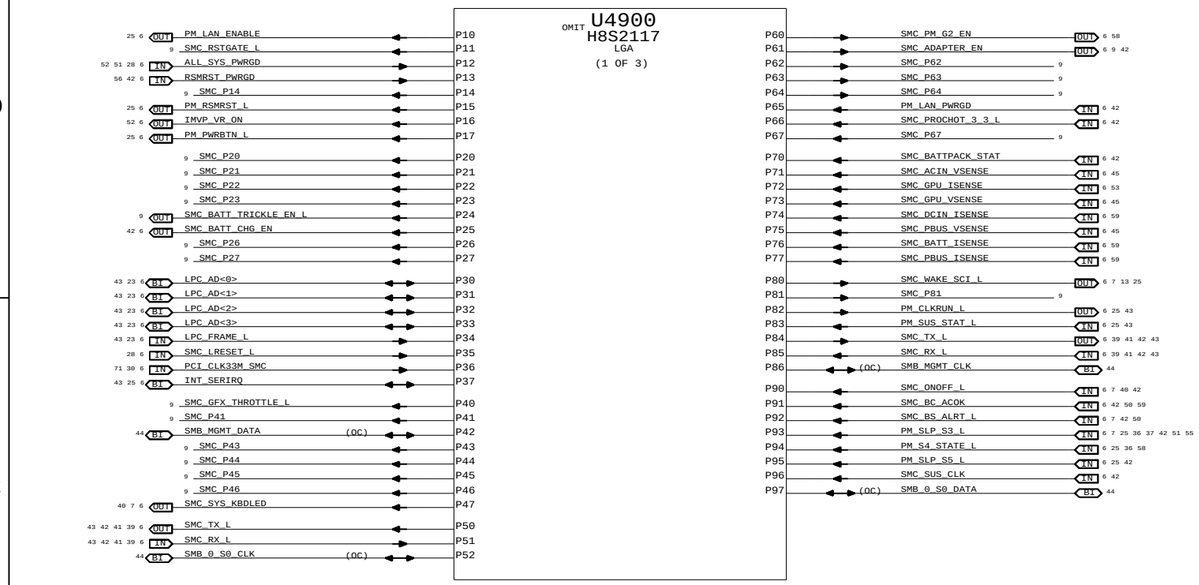
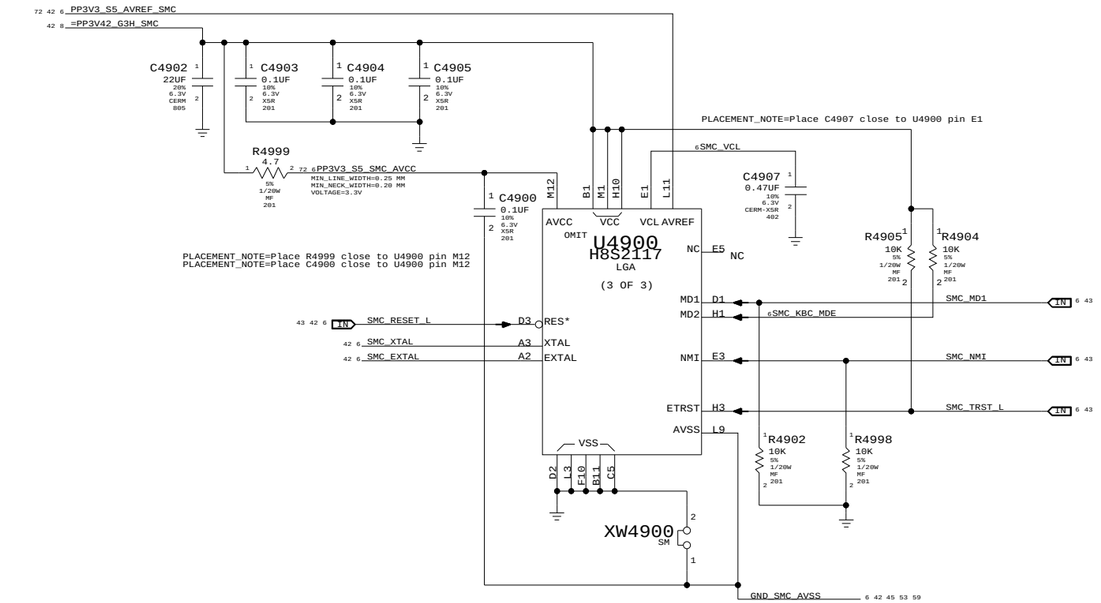
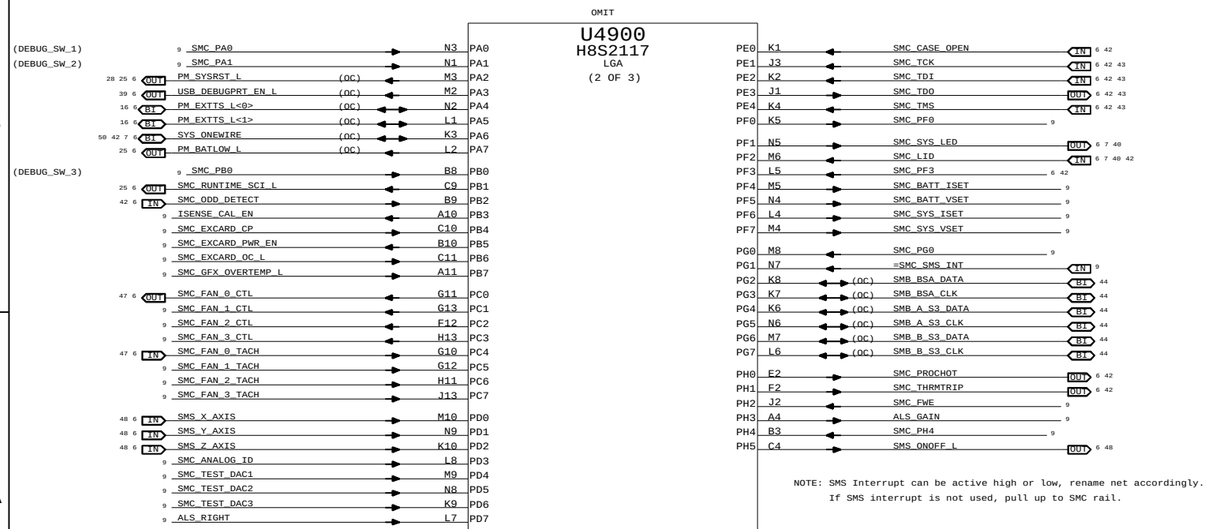
SMC

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.







NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SMC

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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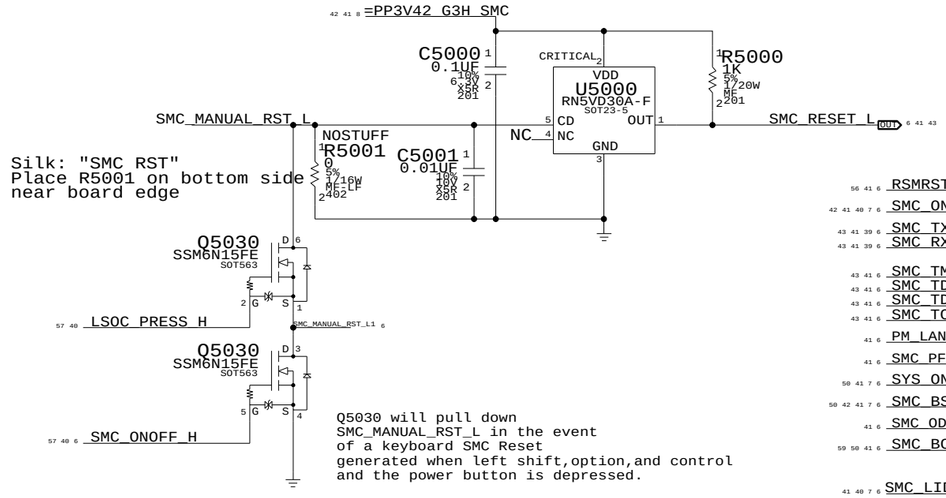
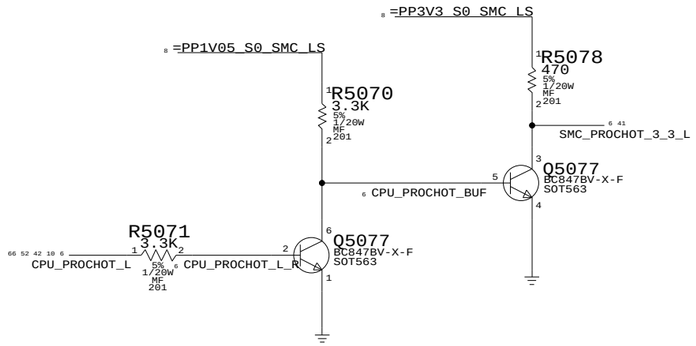
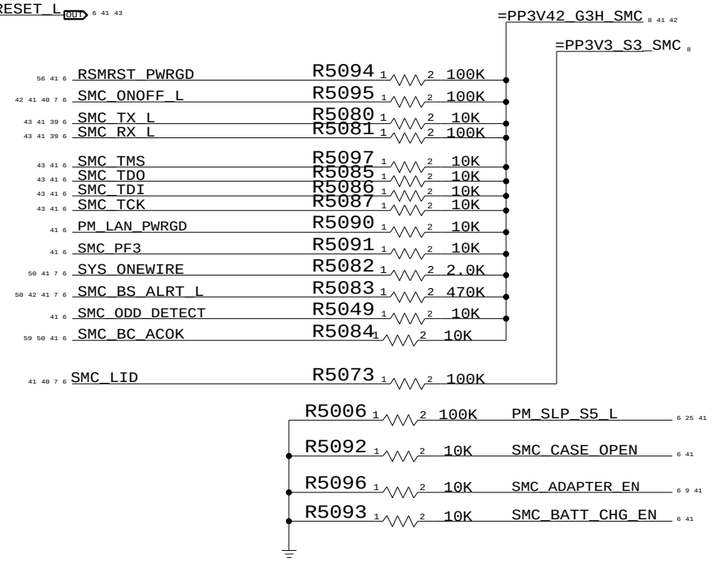
SMC Reset Button / Brownout Detect

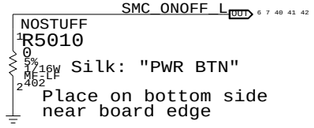


SMC 1.05V to 3.3V Level Shifting

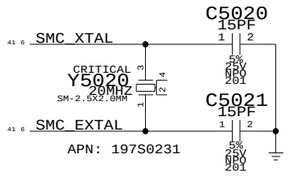




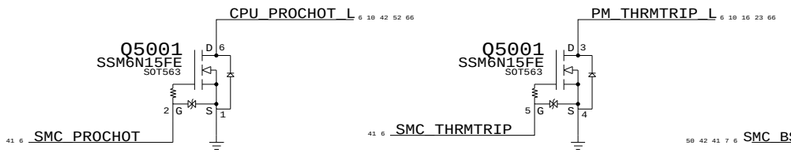
Debug Power Button



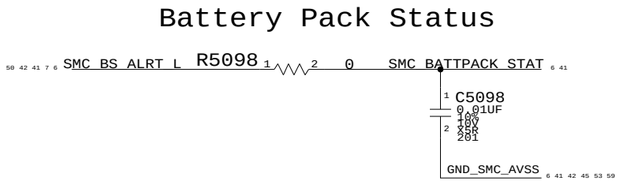
SMC Crystal Circuit



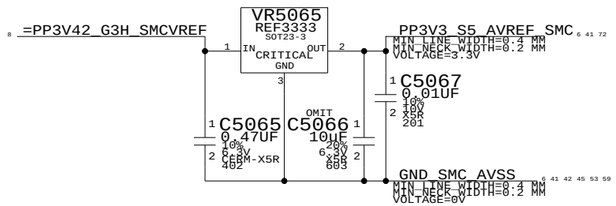
SMC 3.3V to 1.05V Level Shifting



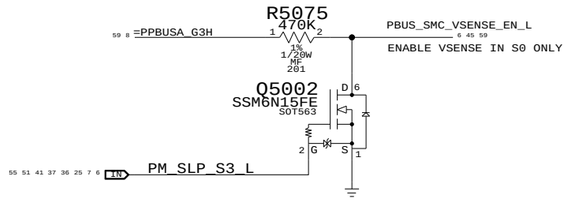
Battery Pack Status

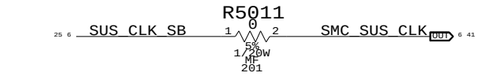


SMC AVREF Supply



3.3V TO PBUS LEVEL SHIFTING





R5011 CLOSE TO SB

SMC SUPPORT

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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D	051-7230	J
SCALE: NONE	SHT 50 OF 109	

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LPC+SPI Connector

CRITICAL
LPCPLUS
J5100
55909-0374
M-ST-SM

516S0573

=PP3V42_G3H_LPCPLUS
=PP5V_S0_LPCPLUS

Place R5101 close to J5100
R5101
47
5%
1/20W
MF
201

SPI_A_SI_R (IN) → SPI_EXT_A_SI_R

Pin	Net	Dir
1	PCI_CLK33M_LPCPLUS	IN
3	LPC_AD<0>	BI
4	LPC_AD<2>	BI
5	LPC_AD<1>	BI
6	LPC_AD<3>	BI
9	BOOTROM_OVR_EN_L	IN
10	SPI_SO	OUT
11	SPI_EXT_A_SCLK_R	
12	LPC_FRAME_L	IN
13	SPI_EXT_CE_L<0>	
14	PM_CLKRUN_L	OUT
15	INT_SERIRQ	BI
16	SMC_TMS	OUT
17	PM_SUS_STAT_L	IN
18	DEBUG_RESET_L	IN
19	SMC_TDI	IN
20	SMC_TDO	OUT
21	SMC_TCK	IN
22	SMC_TRST_L	IN
23	SMC_RESET_L	OUT
24	SMC_MD1	OUT
25	SMC_NMI	OUT
26	SMC_TX_L	IN
27	SMC_RX_L	OUT
28	FRANKCARD_GPIO	OUT

Place R5102 close to J5100
R5102
47
5%
1/20W
MF
201
SPI_A_SCLK_R (IN)

SPI_CS MUX

Pullup to internal ROM on S5
=PP3V3_S5_ROM
=PP3V42_G3H_LPCPLUS
LPCPLUS
R5151
20K
5%
1/20W
MF
201
LPCPLUS
C5150
0.1UF
10%
6.3V
X5R
201
U5150
NC7SB3157P6X
MICROPAK
CRITICAL
LPCPLUS
VCC
GND
SPI_INT_CE_L<0> (OUT)
BOOTROM_OVR_EN_L (IN)
SPI_CE_L<0> (IN)

Place halfway between SPIROM and J5100

NO STUFF
R5152
15
5%
1/20W
MF
201
SPI_CE_R_L<1> (IN)

Place within 0.5" of SB

LPC+SPI Debug Connector

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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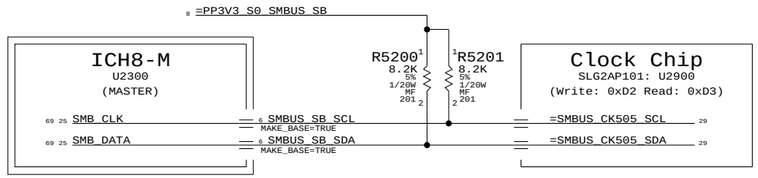
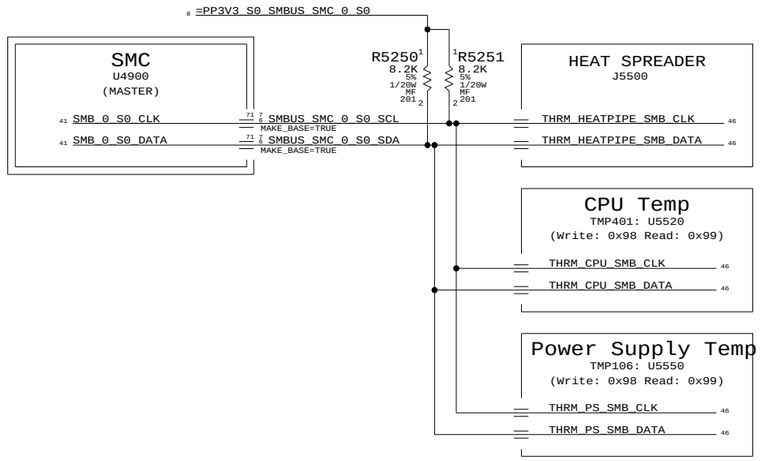
ICH8-M SMBus Connections

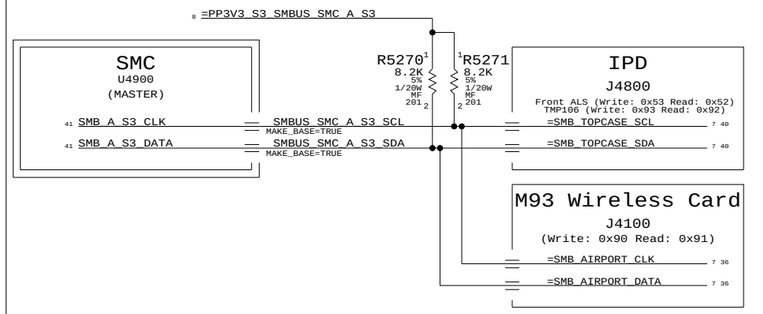


SMC "0" SMBus Connections

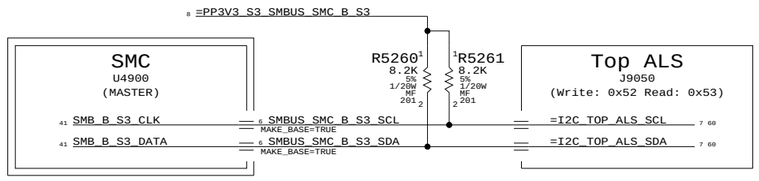


SMC "A" SMBus Connections

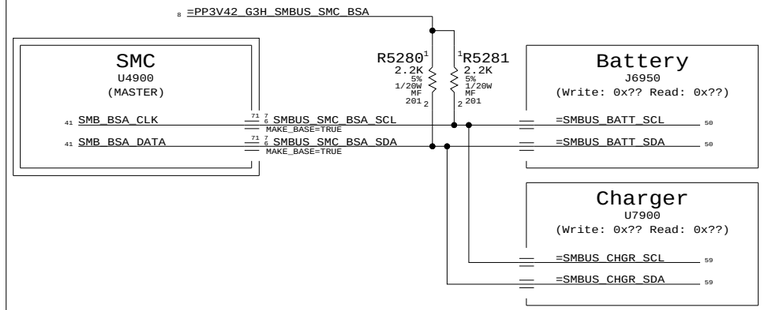
NOTE: SMC RMT bus remains powered and may be active in S3 state



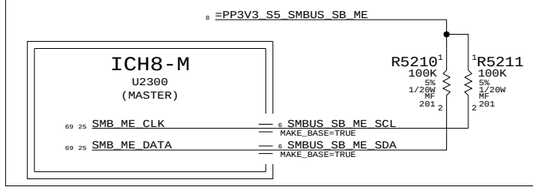
SMC "B" SMBus Connections



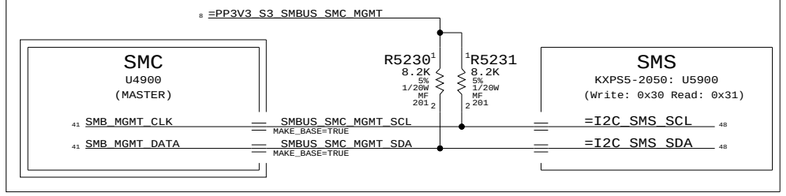
SMC "Battery A" SMBus Connections



ICH8-M ME SMBus Connections



SMC "Management" SMBus Connections



SMBUS CONNECTIONS

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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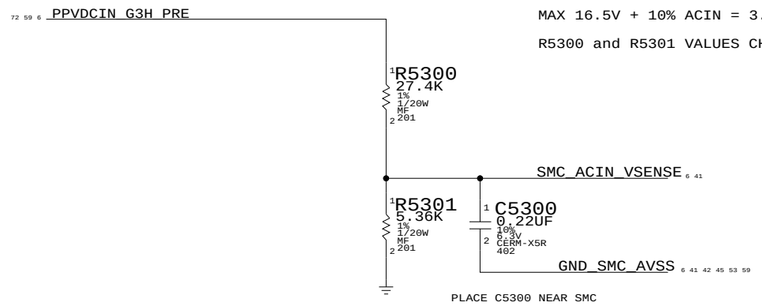
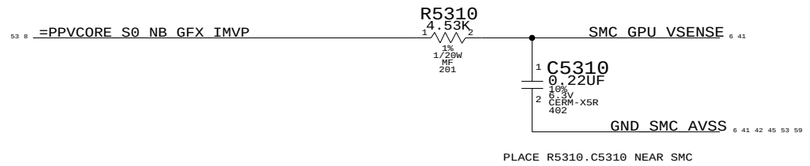
ACIN VOLTAGE SENSE



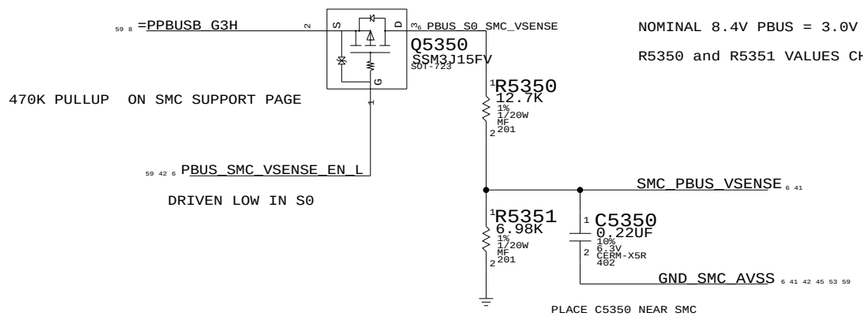
MAX 16.5V + 10% ACIN = 3.0V SMC_PBUS_VSENSE

R5300 and R5301 VALUES CHOSEN FOR RC FILTER @ 4.53KOHM THEVENIN RESISTANCE

GPU VOLTAGE SENSE



PBUS VOLTAGE SENSE



NOMINAL 8.4V PBUS = 3.0V SMC_PBUS_VSENSE

R5350 and R5351 VALUES CHOSEN FOR RC FILTER @ 4.53KOHM THEVENIN RESISTANCE

Voltage Sensors

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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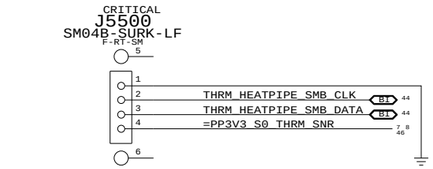
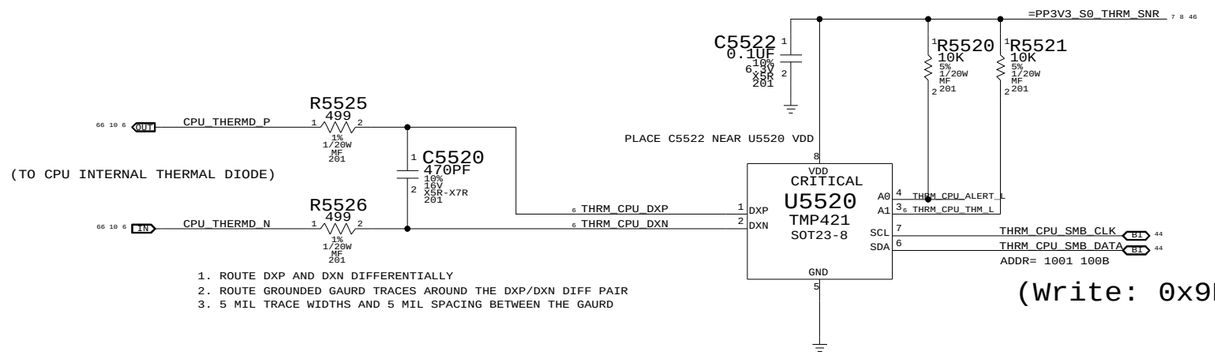
REMOTE TEMP AT HEAT SPREADER



APN:518S0354

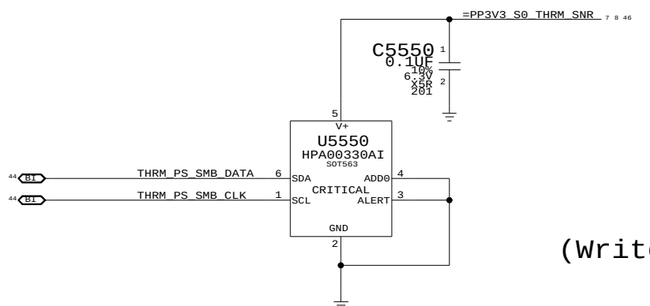
CPU THERMAL DIODE



1. ROUTE DXP AND DXN DIFFERENTIALLY
2. ROUTE GROUNDED GAURD TRACES AROUND THE DXP/DXN DIFF PAIR
3. 5 MIL TRACE WIDTHS AND 5 MIL SPACING BETWEEN THE GAURD

(Write: 0x9E Read: 0x9F)

LOCAL TEMP NEAR POWER SUPPLIES



(Write: 0x90 Read: 0x91)

TEMPERATURE SENSORS

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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SCALE	SHT	OF
NONE	55	109

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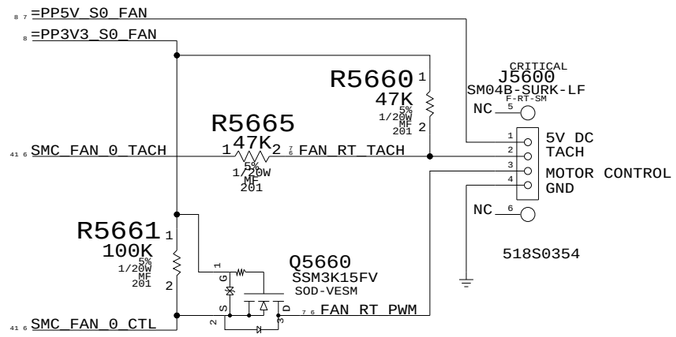
FAN CONNECTOR



Fan

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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SCALE NONE

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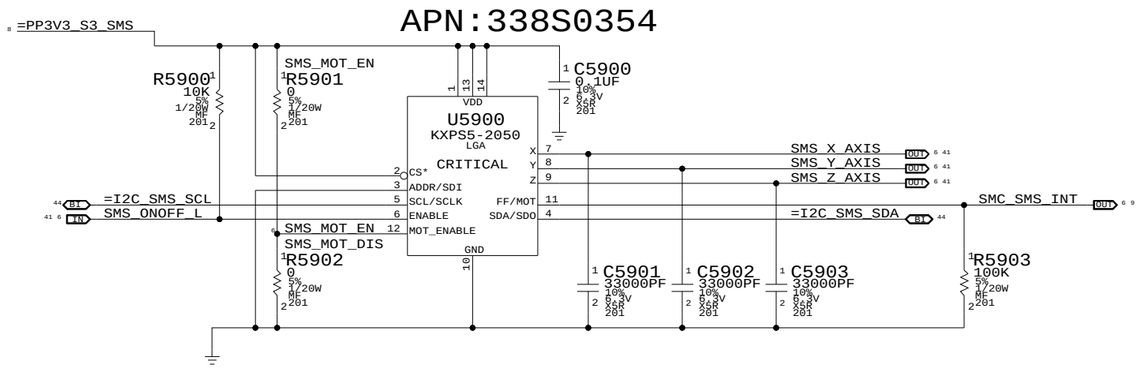
SUDDEN MOTION SENSOR

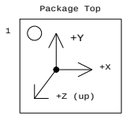
APN:338S0354



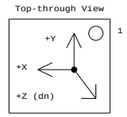
I2C addresses:

ADDR low => 0x30, 0x31
ADDR high => 0x32, 0x33
Alias SCL/SDA to GND if using analog outputs only

Desired orientation when placed on board top-side:



Desired orientation when placed on board bottom-side:



Sudden Motion Sensor (SMS)

SYNC_MASTER=M76_MLB SYNC_DATE=01/12/2007

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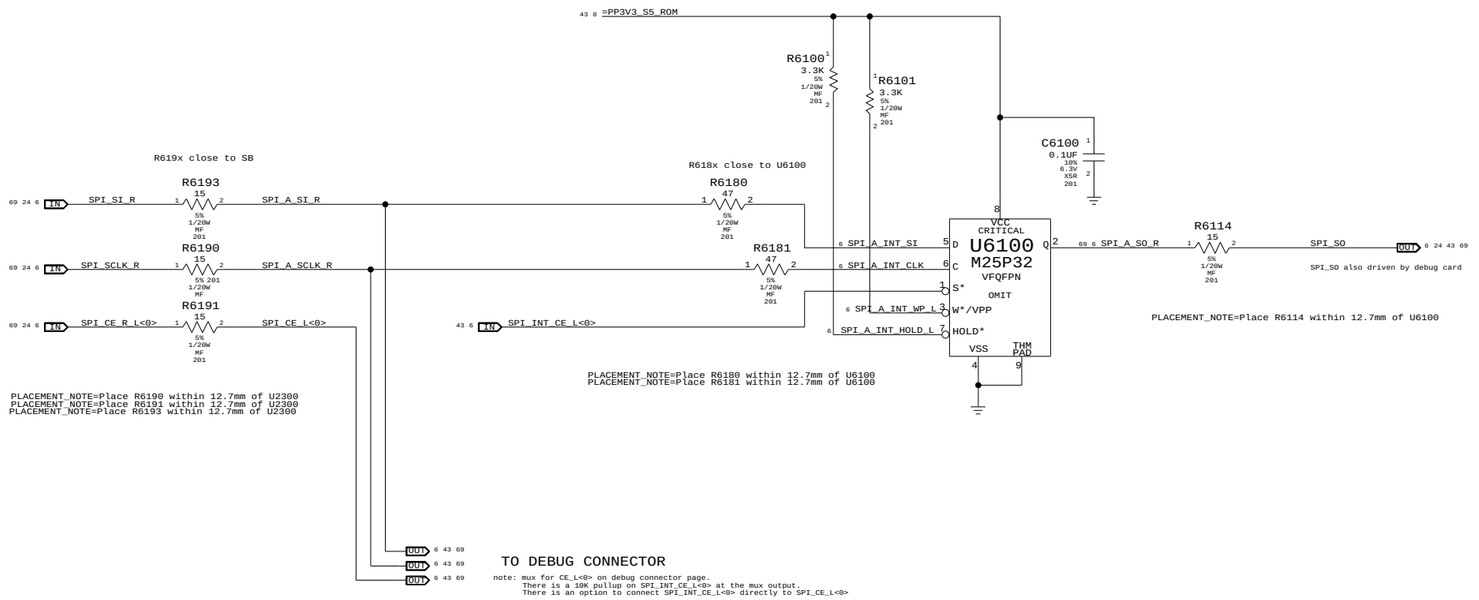
SPI ROM



SPI ROMs

SYNC_MASTER=WFERRY SYNC_DATE=04/26/2006

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D	051-7230	J

SCALE	SHT	OF
NONE	61	109

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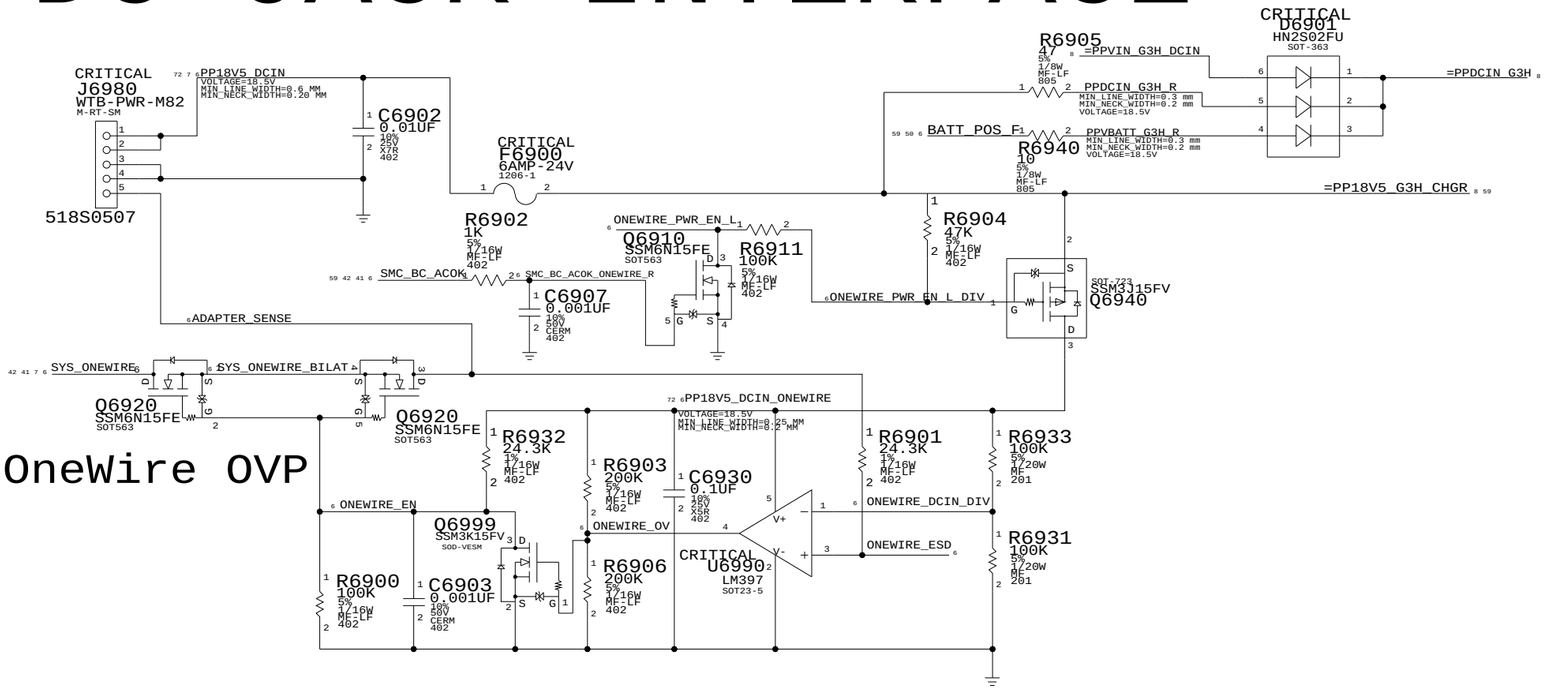
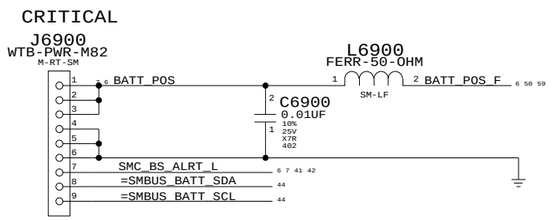
DC-JACK INTERFACE



BATTERY INTERFACE



DC-In & Battery Connectors

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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SCALE	SHT	OF
NONE	69	109

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S0 FETS & POWER SEQUENCING & PGOOD

5V S0 FET

MOSFET	FDM6296
CHANNEL	N-TYPE
RDS(ON)	15 mOhm @4.5V
LOADING	4.061 A

3.3V S0 FET

MOSFET	FDC655BN
CHANNEL	N-TYPE
RDS(ON)	33 mOhm @4.5V
LOADING	1.063 A

3.3V S0 FET

MOSFET	FDC655BN
CHANNEL	N-TYPE
RDS(ON)	33 mOhm @4.5V
LOADING	.776 A

1.8V S0 FET

MOSFET	FDC655BN
CHANNEL	N-TYPE
RDS(ON)	33 mOhm @4.5V
LOADING	1.120 A

1.05V S0 RUN/SS CONTROL

1.25V S0 RUN/SS CONTROL

1.5V S0 RUN/SS CONTROL

DEASSERTED 160MS
AFTER UVLO_D VALID

~26MS

U7002.3 has int 90K pull-up

STUFF R7013,R7014 and UNSTUFF U7002,C7001,C7002
TO USE WIRE-AND OF ALL PGOODs INSTEAD OF TPS3808

S0 FETS & Power Sequencing

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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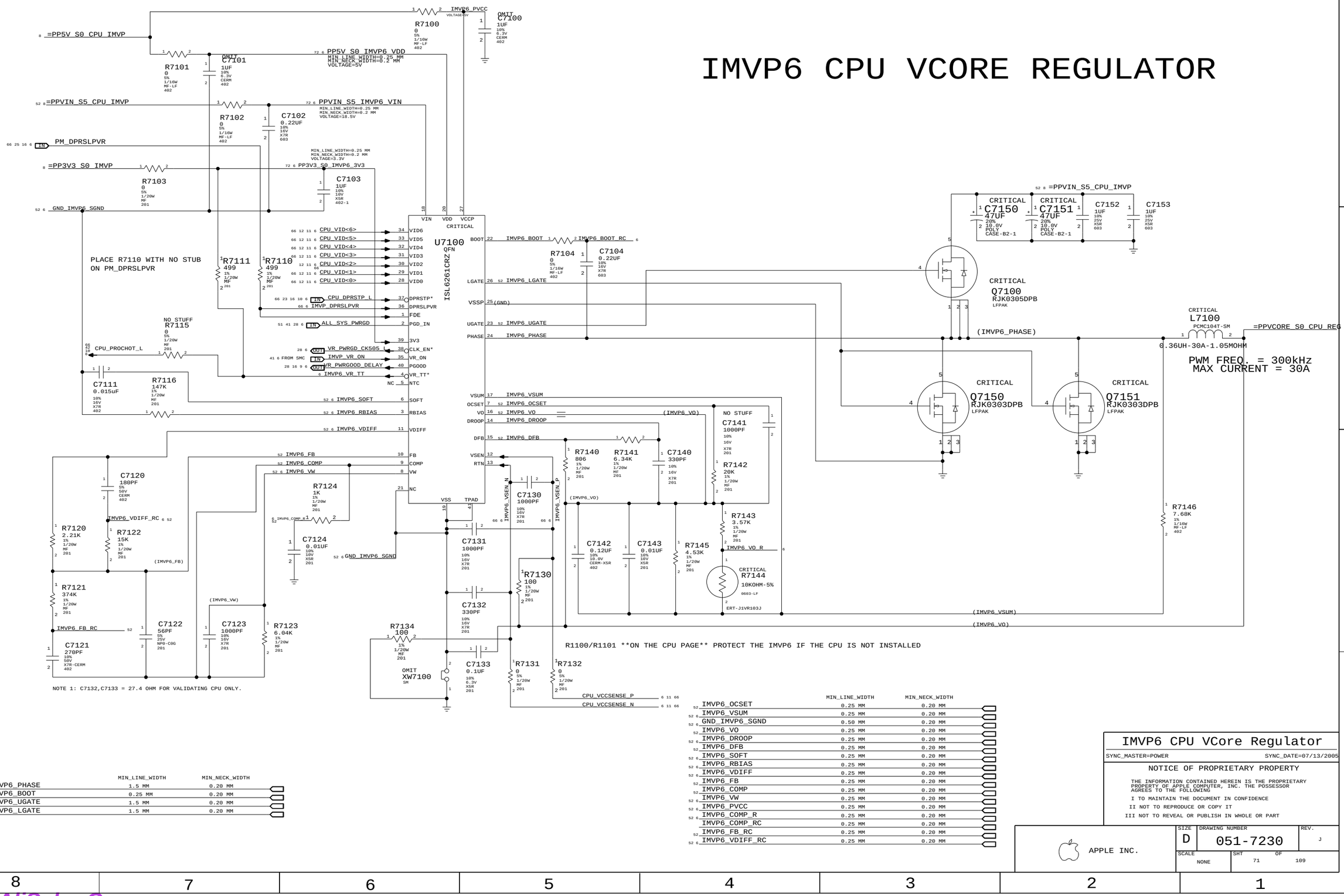
IMVP6 CPU VCORE REGULATOR



	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE	1.5 MM	0.20 MM
IMVP6_BOOT	0.25 MM	0.20 MM
IMVP6_UGATE	1.5 MM	0.20 MM
IMVP6_LGATE	1.5 MM	0.20 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.20 MM
IMVP6_PVCC	0.25 MM	0.20 MM
IMVP6_COMP_R	0.25 MM	0.20 MM
IMVP6_COMP_RC	0.25 MM	0.20 MM
IMVP6_FB_RC	0.25 MM	0.20 MM
IMVP6_VDIFF_RC	0.25 MM	0.20 MM

IMVP6 CPU VCore Regulator

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

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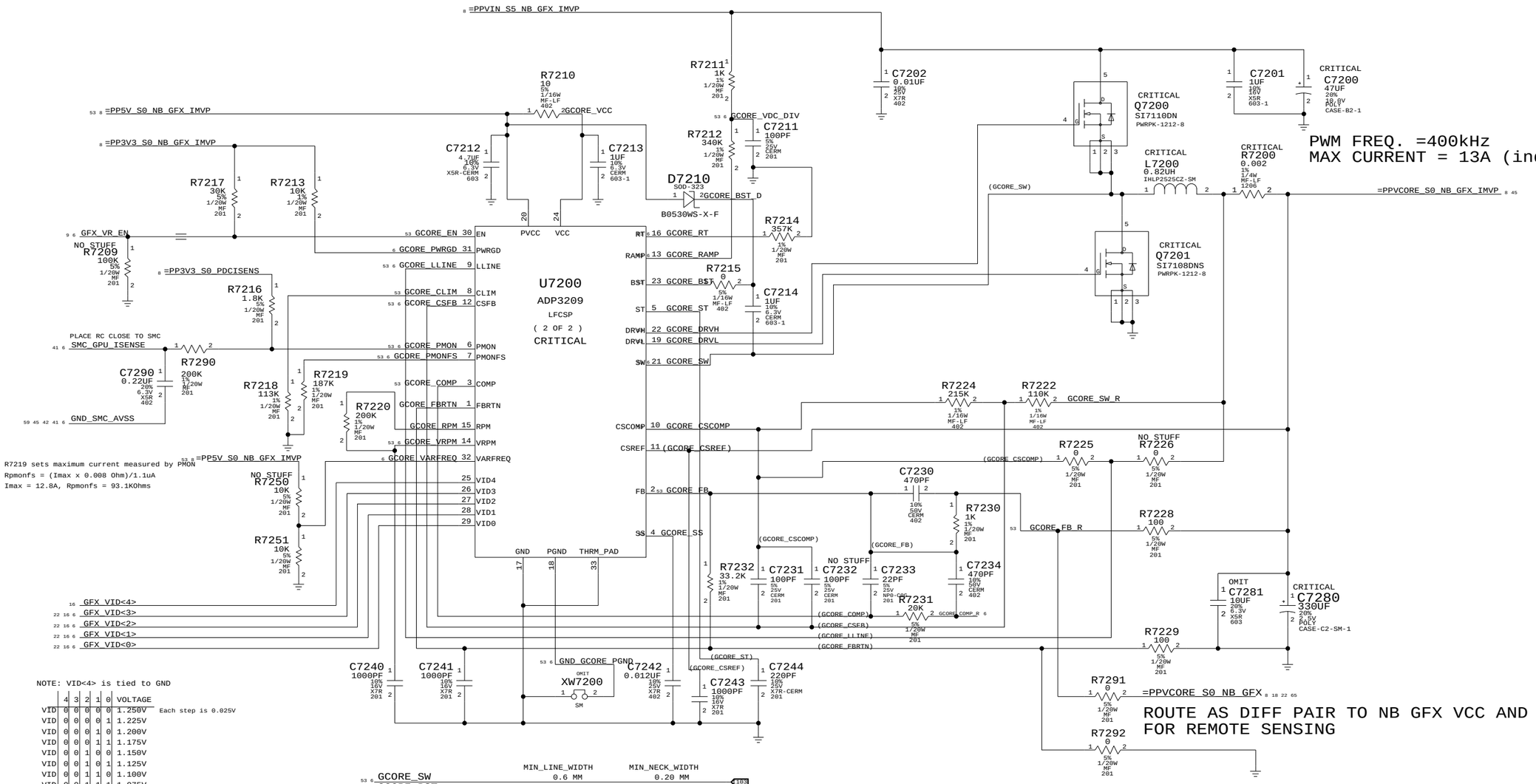
RENDER VCORE POWER SUPPLY



R7219 sets maximum current measured by PMON
Rpmonfs = (Imax x 0.008 Ohm)/1.1uA
Imax = 12.8A, Rpmonfs = 93.1KOhms

NOTE: VID<4> is tied to GND

	4	3	2	1	0	VOLTAGE
VID	0	0	0	0	0	1.250V
VID	0	0	0	0	1	1.225V
VID	0	0	0	1	0	1.200V
VID	0	0	0	1	1	1.175V
VID	0	0	1	0	0	1.150V
VID	0	0	1	0	1	1.125V
VID	0	0	1	1	0	1.100V
VID	0	0	1	1	1	1.075V
VID	0	1	0	0	0	1.050V
VID	0	1	0	0	1	1.025V
VID	0	1	0	1	0	1.000V
VID	0	1	0	1	1	0.975V
VID	0	1	1	0	0	0.950V
VID	0	1	1	0	1	0.925V
VID	0	1	1	1	0	0.900V
VID	0	1	1	1	1	0.875V

Each step is 0.025V

	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
GCORE_SW	0.6 MM	0.20 MM	W103
GCORE_BST	0.3 MM	0.20 MM	W104
GCORE_DRVH	0.6 MM	0.20 MM	W105
GCORE_DRVL	0.6 MM	0.20 MM	W106
GCORE_BST_D	0.3 MM	0.20 MM	W107
GND_GCORE_PGND	0.6 MM	0.20 MM	W108
GCORE_VDC_DIV	0.3 MM	0.20 MM	W110
GCORE_RAMP	0.3 MM	0.20 MM	W111
GCORE_CLIM	0.3 MM	0.20 MM	W112
GCORE_SS	0.3 MM	0.20 MM	W113
GCORE_ST	0.3 MM	0.20 MM	W114
GCORE_SW_R	0.6 MM	0.20 MM	W225

	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
GCORE_CSCOMP	0.3 MM	0.20 MM	W115
GCORE_CSFB	0.3 MM	0.20 MM	W117
GCORE_LLINE	0.3 MM	0.20 MM	W118
GCORE_RT	0.3 MM	0.20 MM	W119
GCORE_EN	0.3 MM	0.20 MM	W120
GCORE_COMP	0.3 MM	0.20 MM	W121
GCORE_FB	0.3 MM	0.20 MM	W122
GCORE_FBRTN	0.3 MM	0.20 MM	W123
GCORE_PMON	0.3 MM	0.20 MM	W124
GCORE_PMONFS	0.3 MM	0.20 MM	W125
GCORE_RPM	0.3 MM	0.20 MM	W126
GCORE_VRPM	0.3 MM	0.20 MM	W128
GCORE_FB_R	0.3 MM	0.20 MM	W226

Render VCore Supplies

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE: NONE	SHT 72 OF 109	

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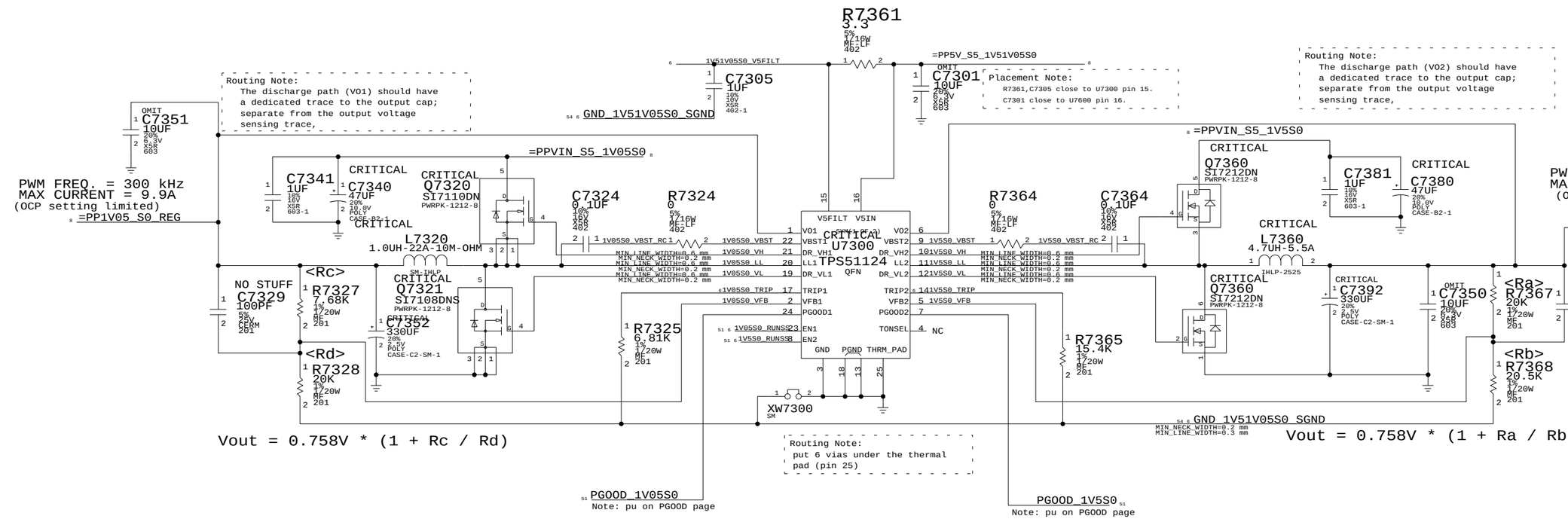
1.5V/1.05V POWER SUPPLY

State	PM_SLP_S3_L	PP1V5_S0	PP1V05_S0
S0	HIGH	1.5V	1.05V
S3/S5/G3Hot	LOW	0.0V	0.00V



1.5V/1.05V Supplies

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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D	051-7230	J
SCALE: NONE	SHT 73 OF 109	

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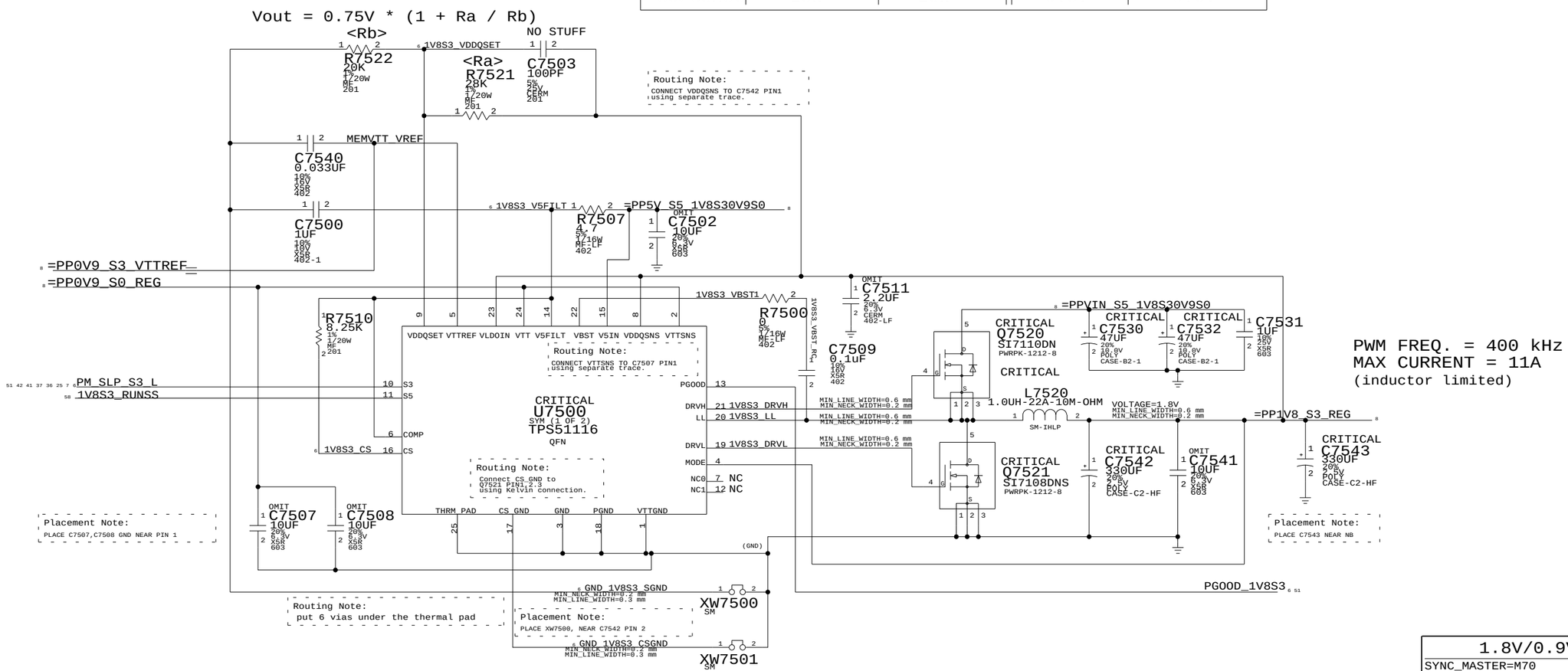
1.8V/0.9V POWER SUPPLY

State	PM_S4_STATE_L	PM_SLP_S3_L	PP1V8_S3	PP0V9_S0
S0	HIGH	HIGH	1.8V	0.9V
S3	HIGH	LOW	1.8V	0.0V
S5/G3Hot	LOW	LOW	0.0V	0.0V



1.8V/0.9V Supplies

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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SCALE	SHT	OF
NONE	75	109

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5V/3.3V POWER SUPPLY

State	SMC_PM_G2_EN	PP3V3_G3H	PP5V_S5	PP3V3_S5
G3H	LOW	3.3V	0.0V	0.0V
S0/S3/S5	HIGH	3.3V	5.0V	3.3V

Vout = 1V * (1 + Ra / Rb)
5.120V = 1V * (1 + 17.8K / 4.32K)

<Ra> R7667 17.8K 1% 1/20W MF 201
<Rb> R7668 4.32K 1% 1/20W MF 201
NO STUFF C7667 100PF 5% 25V CERM 201
GND_5V3V3S5_SGND
5VS5_FB
R7610 0 5% 1/16W MF 402
C7600 0.001UF 10% 50V CERM 402
25V3V3S5_VREF
5V3V3S5_V5FILT
Routing Note: The discharge path (VO1) should have a dedicated trace to the output cap;
Routing Note: The discharge path (VO2) should have a dedicated trace to the output cap; separate from the output voltage sensing trace,

=PPVIN_S5_5VS5
C7680 47UF 20% 10.0V POLY CASE-B2-1
C7681 1UF 10% 16V X5R 603-1
Routing Note: put 6 vias under the thermal pad (pin 33)
CRITICAL U7600 TPS51120 LLP SYM (2 OF 3)
C7660 0.1UF 10% 16V X5R 402
R7660 0 5% 1/16W MF-LF 402
RSMRST_PWRGD
5VS5_RUNSS
5VS5_VBST_RC
5VS5_DRVH
5VS5_LL
5VS5_DRVL
CRITICAL Q7660 SI7110DN PWRPK-1212-8
CRITICAL L7660 3.3UH-6.5A IHLP
VOLTAGE=5V MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.2 mm
C7690 10UF 20% 6.3V X5R 603
CRITICAL C7691 150UF 20% 6.3V POLY CASE-B2-HF
CRITICAL C7692 150UF 20% 6.3V POLY CASE-B2-HF
CRITICAL Q7661 SI7110DN PWRPK-1212-8
R7605 5.90K 1% 1/20W MF 201
R7603 7.15K 1% 1/20W MF 201
5V3V3S5_V5FILT
=PPVIN_S5_5VS5
R7601 4.7 5% 1/16W MF-LF 402
5V3V3S5_VREG3
C7602 1UF 10% 16V X5R 603-1
C7604 10UF 20% 6.3V X5R 603
C7605 1UF 10% 16V X5R 402-1
C7603 10UF 20% 6.3V X5R 603
XW7601 SM
GND_5V3V3S5_SGND MIN_NECK_WIDTH=0.2 mm MIN_LINE_WIDTH=0.3 mm

Placement Note:
R7601,C7605 close to U7600 pin 20.
C7602 close to U7600 pin 22.
C7604 close to U7600 pin 21.
C7603 CLOSE TO U7600 PIN 19.
R7605,R7603 close to U7600.

PWM FREQ. = 280 kHz
MAX CURRENT = 6.0A
(inductor limited)
=PP5V_S5_REG

=PPVIN_S5_3V3S5
C7641 1UF 10% 16V X5R 603-1
CRITICAL C7640 47UF 20% 10.0V POLY CASE-B2-1
C7620 0.1UF 10% 16V X5R 402
R7620 0 5% 1/16W MF-LF 402
3V3S5_RUNSS
3V3S5_VBST
3V3S5_DRVH
3V3S5_LL
3V3S5_DRVL
CRITICAL Q7620 SI7110DN PWRPK-1212-8
CRITICAL L7620 2.2UH-14A IHLP2525CZ-SM1
VOLTAGE=3.3V MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.2 mm
CRITICAL Q7621 SI7110DN PWRPK-1212-8
CRITICAL C7652 150UF 20% 6.3V POLY CASE-B2-HF
CRITICAL C7651 150UF 20% 6.3V POLY CASE-B2-HF
C7650 10UF 20% 6.3V X5R 603

PWM FREQ. = 430 kHz
MAX CURRENT = 7.8A
(OCP setting limited)
=PP3V3_S5_REG

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7682,C7680	KEMET T520V336M016ATE0457650
128S0093	128S0092	?	C7640	KEMET T520V336M016ATE0457650

5V/3.3V Supplies
SYNC_MASTER=M70 SYNC_DATE=02/01/2007

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APPLE INC.
SIZE D | DRAWING NUMBER 051-7230 | REV. J
SCALE NONE | SHT 76 OF 109

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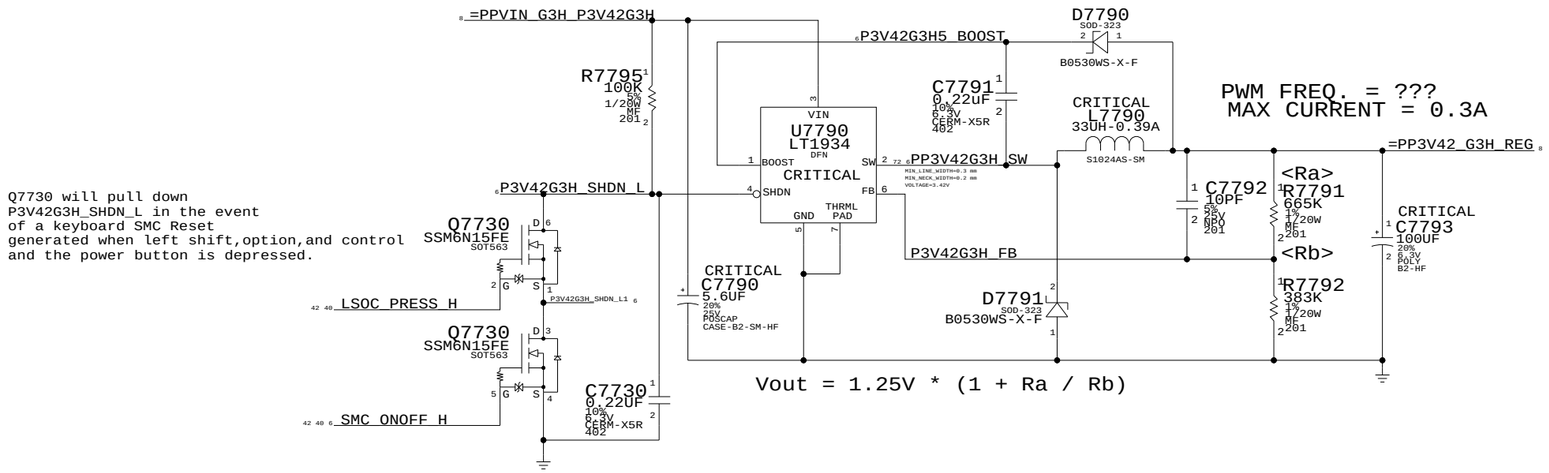
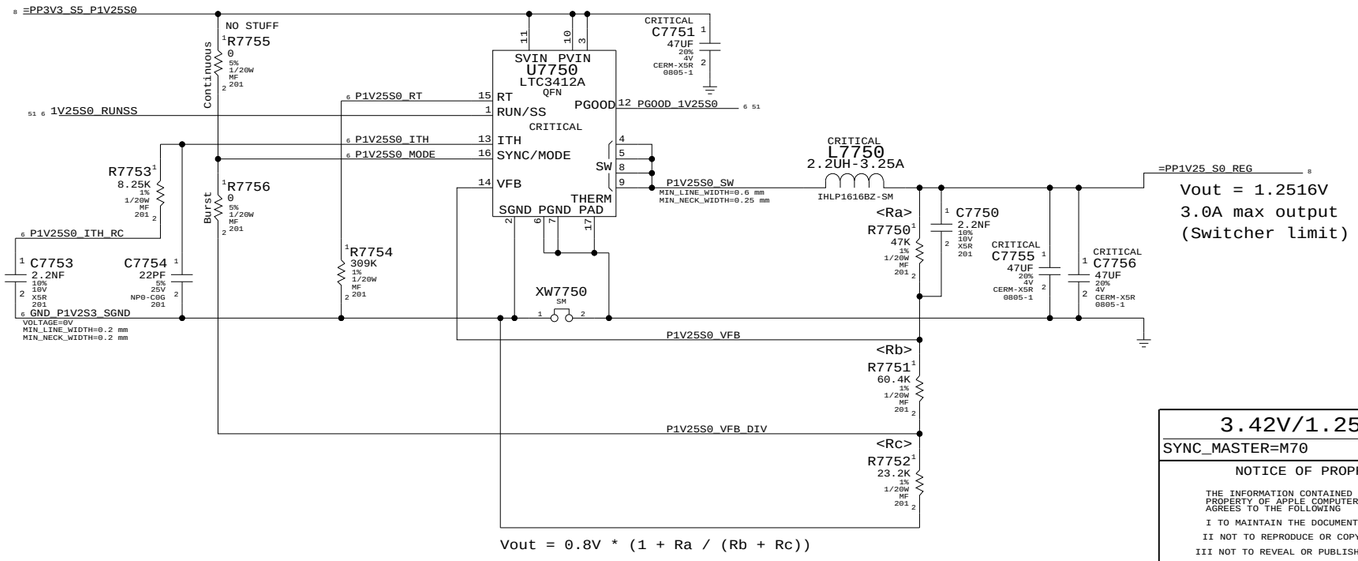
3.425V G3H SUPPLY

Supply needs to guarantee 3.31V delivered to SMC VRef generator



1.25V S0 REGULATOR



3.42V/1.25V Switcher		
SYNC_MASTER=M70	SYNC_DATE=01/09/2007	

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	D	051-7230	J
	SCALE: NONE	SHT 77 OF 109	

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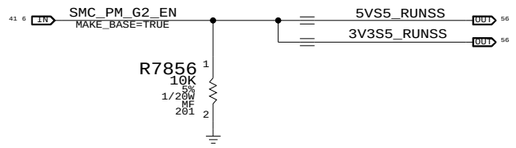
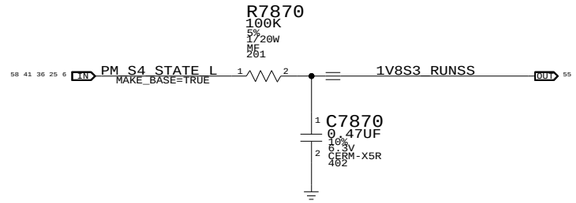
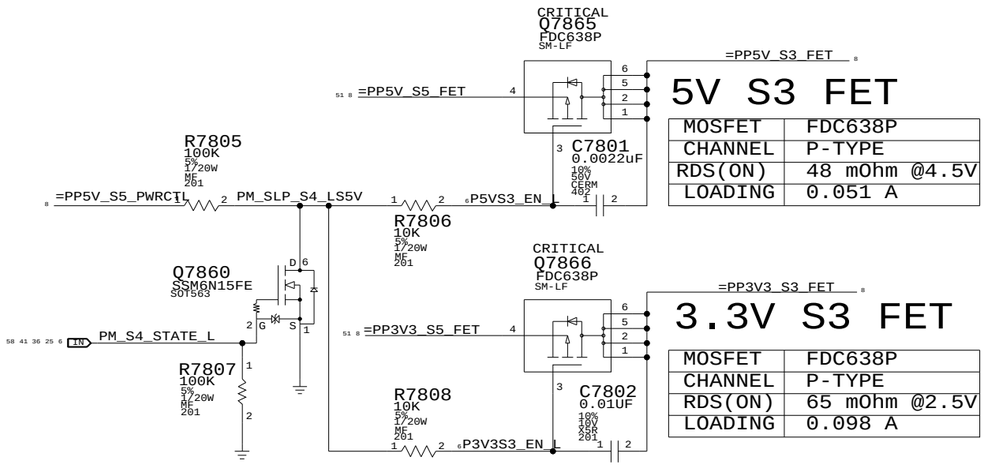
S3 FETS & S3/S5 CONTROL

5V/3.3V S5 RUN/SS CONTROL



1.8V S3 RUN/SS CONTROL





5V S3 FET

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.051 A

3.3V S3 FET

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	65 mOhm @2.5V
LOADING	0.098 A

S3 FET & S3/S5 Control

SYNC_MASTER=M70 SYNC_DATE=02/01/2007

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 78 OF 109	

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PBUS SUPPLY / BATTERY CHARGER

PBUS CURRENT SENSOR

=PPBUSB_G3H
R7981 21 1% 1/10W MF-LF 402
C7980 0.1UF 10% 16V X5R 402
U7980 LTC6102AP DFN
V+ -INF -INS +IN V- OUT VREG SHDN THM PAD
6 PBUS_ISENSE_VREG
6 PBUS_ISENSE_IN_NEG
=PPBUSA_G3H
PLACE C CLOSE TO SMC
SMC_PBUS_ISENSE 6 41
R7989 4.53K 1% 1/20W MF 201
C7989 0.22UF 20% 6.3V X5R 402
GND_SMC_AVSS 6 41 42 45 53 59
45 42 6 PBUS_SMC_VSENSE_EN_L
LTC6102 DISABLED WHEN SHDN=1
LTC6102 ENABLED WHEN SHDN=0

=PPBUSB_G3H 59 45 8
=PPBUSA_G3H 59 42 8
=PP18V5_G3H_CHGR 50 8
=PP3V42_G3H_CHGR 59 8
CHGR_DCIN 59 6
GND_CHGR_SGND 59 6

CRITICAL Q7900 AO4409 SO1
CRITICAL Q7901 AO4409 SO1
PPVDCIN_G3H_PRE2 MIN_LINE_WIDTH=0.2 MM MIN_NECK_WIDTH=0.2 MM
PPVDCIN_G3H_PRE MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 MM
CRITICAL D7910 SOD-323 B0530WS-X-F
C7900 0.1UF 10% 25V X5R 402
R7900 100K 5% 1/20W MF 201
R7999 100K 5% 1/20W MF 201
CHGR_SGATE_DIV
R7962 62K 5% 1/20W MF 201
R7960 57.6K 1% 1/20W MF 201
R7961 1.82K 1% 1/20W MF 201
C7960 0.1UF 10% 25V X5R 402
CHGR_AMON
CHGR_LOWCURRENT_GATE
CHGR_LOWCURRENT_REF
CRITICAL U7960 TL331 SOT23-5
C7910 0.1UF 10% 25V X5R 402
R7901 62K 5% 1/20W MF 201
CHGR_SGATE
R7923 10 5% 1/20W MF 201
XW7920 SM
XW7921 SM
C7924 0.047UF 10% 16V X7R 402
R7921 10 5% 1/20W MF 201
CRITICAL R7920 0.02 1% 1W MF 0612
R7910 30.1K 1% 1/20W MF 201
R7911 9.76K 1% 1/20W MF 201
(CHGR_ACIN)
CHGR_VDD
CHGR_VDDP
R7940 4.7 5% 1/10W MF-LF 402
C7940 1UF 10% 10V X5R 402-1
C7941 1UF 10% 10V X5R 402-1
C7947 1UF 10% 10V X5R 402-1
C7995 0.1UF 10% 25V X5R 402
C7996 0.1UF 10% 25V X5R 402
CRITICAL U7900 ISL6258 QFN
VDD VDDP VHST SCL SDA VREF ACIN ICOMP VCOMP VNEG CSOP CSON AGATE CSIP CSIN BGATE DCIN BOOT UGATE PHASE LGATE TRKL* AMON BMON ACOK THRM_PAD AGND PGND
OMIT
CHGR_SCL
CHGR_SDA
pullups offpage
CHGR_AGATE
CHGR_CSIP
CHGR_CSIN
CHGR_BGATE
CHGR_DCIN 6 59
CHGR_BOOT
CHGR_UGATE
CHGR_PHASE
CHGR_LGATE
NC
CHGR_AMON 6 59
CHGR_BMON 6 59
CHGR_ACOK 6 59
GND_CHGR_SGND 6 59
CRITICAL Q7920 FDM6296 MICROFET3X3
CRITICAL Q7921 FDM6296 MICROFET3X3
C7925 0.1UF 10% 25V X5R 402
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 MM
PP18V5_S5_CHGR_SW_R 72 6
CRITICAL C7920 22UF 20% 25V POLY CASE-D2-LF
CRITICAL C7921 22UF 20% 25V POLY CASE-D2-LF
C7922 1UF 10% 25V X5R 603
C7923 1UF 10% 25V X5R 603
KELVIN CONNECTION TO CURRENT SENSOR U7980
CRITICAL R7980 0.002 1% 1/4W MF-LF 1206
=PPBUSA_G3H 8 42 59
TO SYSTEM
=PPBUSB_G3H 8 45 59
CRITICAL F7900 7AMP-24V 1206
CRITICAL L7900 4.7UH-7.5A IHLP4040CZ-SM
CRITICAL R7930 0.01 1% 1W MF 0612
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 MM PPVBAT_G3H_CHGR_REG
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 MM PPVBAT_G3H_CHGR_OUT 6 59 72
CRITICAL C7930 47UF 20% 16.0V POLY CASE-B2-1
CRITICAL C7931 47UF 20% 16.0V POLY CASE-B2-1
C7935 1UF 10% 25V X5R 603
XW7930 SM
XW7931 SM
R7931 10 5% 1/20W MF 201
R7947 10 5% 1/20W MF 201
PPVBAT_G3H_CHGR_REG 6 72
PPVBAT_G3H_CHGR_SEL
R7945 56.2K 1% 1/10W MF-LF 402
CHGR_VCOMP_R
C7945 0.001UF 10% 50V CERM 402
C7943 0.1UF 10% 16V X5R 402
C7942 33000PF 10% 6.3V X5R 201
C7944 0.01UF 10% 16V X5R 201
R7946 3.01K 1% 1/10W MF-LF 402
CHGR_VNEG
C7946 470PF 10% 50V CERM 402
XW7900 SM
C7926 1000PF 10% 16V X7R 201
(CHGR_CSOP)
(CHGR_CSON)
PWM FREQ. = 400 kHz
MAX CURRENT = ??A
(??? limited)

AMON PULLDOWN LOGIC

CHGR_AMON 6 59
=PP3V42_G3H_CHGR 59 8
R7974 1M 5% 1/20W MF 201
Q7970 SSM6N15FE SOT563
NO STUFF
R7975 1M 5% 1/20W MF 201
CHGR_VDD 59 6
R7973 1M 5% 1/20W MF 201
Q7970 SSM6N15FE SOT563
CHGR_VDD_L
CHGR_VDD_R

BATTERY CHARGING

CRITICAL Q7950 AO4409 SO1
PPVBAT_G3H_CHGR_OUT 72 59 6
C7950 0.01UF 10% 16V X5R 201
C7951 0.1UF 10% 16V X5R 402
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 MM
BATT_POS_F 6 50
TO BATTERY
CHGR_BGATE 6 59

=SMBUS_CHGR_SCL 44 — CHGR_SCL 59
=SMBUS_CHGR_SDA 44 — CHGR_SDA 59
ACOK pullup/down on SMC page
SMC_BC_ACOK 50 42 41 6 — CHGR_ACOK 59
MAKE_BASE=TRUE

CHGR_BMON 59 6 — R7971 0 5% 1/20W MF 201 — C7972 0.68UF 10% 6.3V CERM 402 — GND_SMC_AVSS 6 41 42 45 53 59
PLACE RC CLOSE TO SMC
SMC_BATT_ISENSE 6 41
CHGR_AMON 59 6 — R7970 0 5% 1/20W MF 201 — C7971 0.68UF 10% 6.3V CERM 402 — GND_SMC_AVSS 6 41 42 45 53 59
PLACE RC CLOSE TO SMC
SMC_DCIN_ISENSE 6 41

APPLE INC.	SIZE D	DRAWING NUMBER 051-7230	REV. J
	SCALE NONE	SHT 79 OF 109	

PBUS Supply/Battery Charger
SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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LCD + CAMERA CONNECTOR

=PP3V3_S5_LCD
R9002 100K 5% 1/20W MF 201
C9040 0.1UF 10% 6.3V X5R 201
Q9004 SSM3K15FV SOD-VESM
R9023 10K 5% 1/20W MF 201
CRITICAL Q9003 FDC638P SM-LF
C9011 0.1UF 10% 16V X7R 201
C9012 10UF 20% 6.3V X5R 603
PP3V3_LCDVDD_SW
VOLTAGE=3.3V MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM
OMIT
C9013 0.0033UF 10% 50V CERM 402
LCDVDD_PWREN_L
LCDVDD_PWREN_L_R
LCDVDD_PLT_RST_L
LVDS_VDD_EN
U9040 TC7SZ08AFEF SOT665
LVDS_VDD_GATED_EN
R9014 100K 1% 1/20W MF 201

CRITICAL L9007 90-OHM-100MA 1210-4SM1
=USB2_CAMERA_N
=USB2_CAMERA_P
CRITICAL L9005 FERR-120-OHM-1.5A 0402-LF
=PP5V_S3_CAMERA
C9016 1000PF 10% 16V X7R 201
CRITICAL L9004 FERR-120-OHM-1.5A 0402-LF
C9015 1000PF 10% 16V X7R 201

L9052 240-OHM-0.2A-0.8-OHM 0201
=I2C_TOP_ALS_SDA
I2C_TOP_ALS_SDA_F
L9051 240-OHM-0.2A-0.8-OHM 0201
=I2C_TOP_ALS_SCL
I2C_TOP_ALS_SCL_F
C9052 10PF 5% 25V NPO 201
C9051 10PF 5% 25V NPO 201

CRITICAL J9000 20347-130E-11 F-RT-SM
518S0433

PLACE FILTERS AND CAPS NEAR PINS ON CONNECTOR

L9008 120-OHM-0.3A-EMI 0402-LF
=PP3V3_S0_LCD
(LVDS_DDC_POWER)
C9010 1000PF 10% 16V X7R 201
R9008 10K 5% 1/20W MF 201
R9009 10K 5% 1/20W MF 201
LVDS_DDC_CLK
LVDS_DDC_DATA

PP5V_S3_CAMERA_F
USB2_CAMERA_F_P
USB2_CAMERA_F_N
PP3V3_LCDVDD_SW_F
PP3V3_S0_LCD_F
CAMERA I/F
LCD I/F

LVDS_A_DATA_F_N<0>
LVDS_A_DATA_F_P<0>
LVDS_A_DATA_F_N<1>
LVDS_A_DATA_F_P<1>
LVDS_A_DATA_F_N<2>
LVDS_A_DATA_F_P<2>
LVDS_A_CLK_F_N
LVDS_A_CLK_F_P
LCDBKLT_RTN<1>
LCDBKLT_RTN<2>
LCDBKLT_RTN<3>
LCDBKLT_RTN<4>
LCDBKLT_RTN<5>
LCDBKLT_RTN<6>
PPVOUT_S0_LCDBKLT

CRITICAL L9010 90-OHM-100MA 1210-4SM1
LVDS_A_DATA_N<0>
LVDS_A_DATA_P<0>
CRITICAL L9011 90-OHM-100MA 1210-4SM1
LVDS_A_DATA_N<1>
LVDS_A_DATA_P<1>
CRITICAL L9012 90-OHM-100MA 1210-4SM1
LVDS_A_DATA_N<2>
LVDS_A_DATA_P<2>
CRITICAL L9006 90-OHM-100MA 1210-4SM1
LVDS_A_CLK_N
LVDS_A_CLK_P

LVDS REFERENCE CURRENT,3.24K OHM PULL DOWN RESISTOR NEEDED
R9013 3.24K 1% 1/20W MF 201
LVDS_IBG
PLACE NEAR NB

MIC CONNECTOR

CRITICAL J9050 GS03067-11131-7F F-RT-SM
PP3V3_S3_MIC_F
NC
NC
GND_MIC_F
L9050 240-OHM-0.2A-0.8-OHM 0201
=PP3V3_S3_MIC
MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.20MM VOLTAGE=3.3V
L9030 240-OHM-0.2A-0.8-OHM 0201
AUD_MIC_DATA_F
AUD_MIC_DATA
L9031 240-OHM-0.2A-0.8-OHM 0201
AUD_MIC_CLK_F
AUD_MIC_CLK
L9053 240-OHM-0.2A-0.8-OHM 0201
C9050 0.01UF 10% 10V X5R 201
C9053 0.01UF 10% 10V X5R 201
C9030 10PF 5% 25V NPO 201 NO STUFF
C9031 10PF 5% 25V NPO 201 NO STUFF

APN:518S0356

LVDS,Camera Conn. and ALS Conn.
SYNC_MASTER=GPU SYNC_DATE=06/23/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 90 OF 109	

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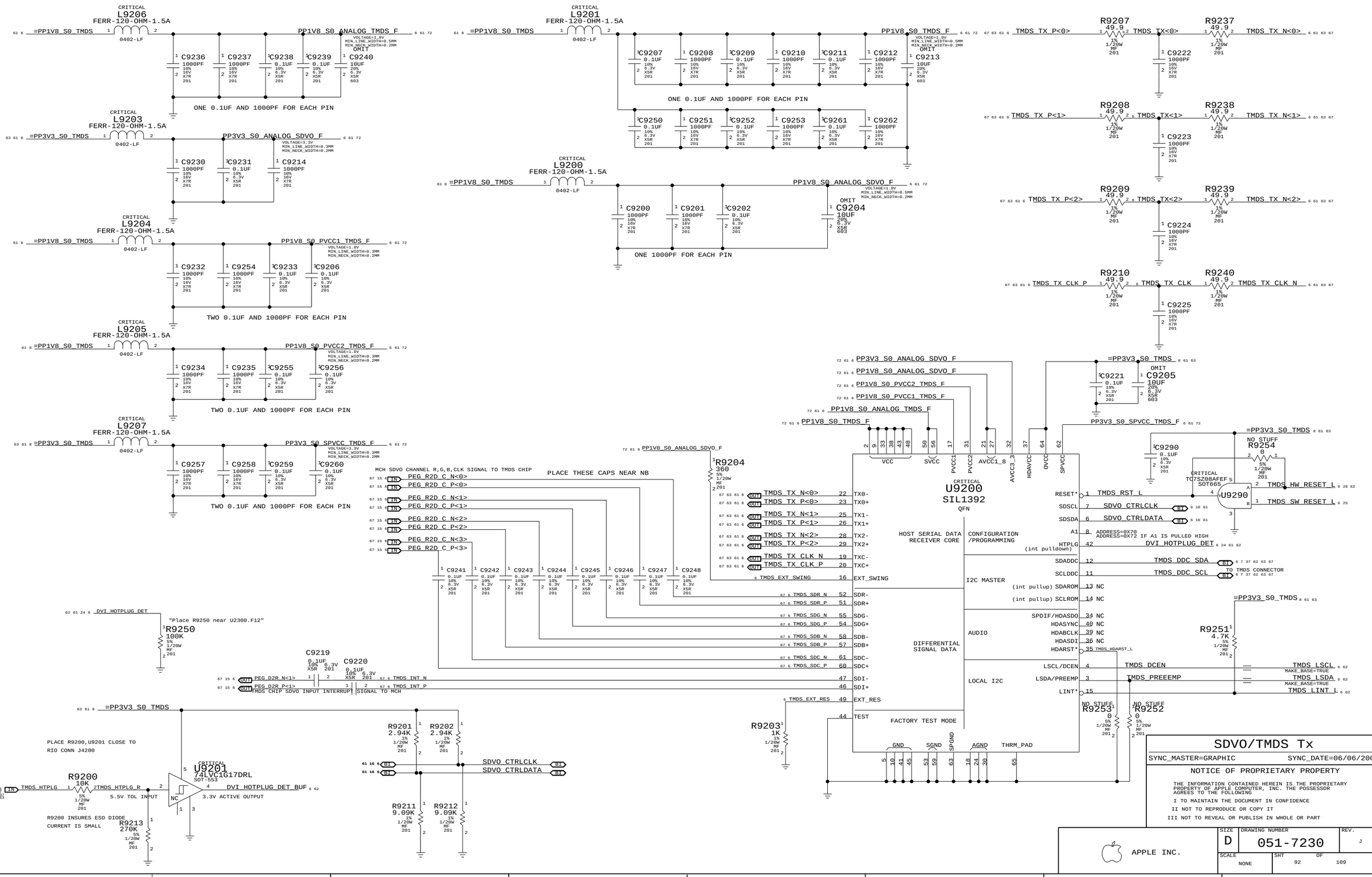

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SST8051 microcontroller for HDCP support

=PP3V3_S0_HDCP

SST8051 C9341 0.1UF 10% 6.3V X5R 201

DVI_HOTPLUG_DET_BUF

SST8051 R9340 10K 5% 1/20W MF 201

SST8051 C9340 1UF 10% 6.3V CERM 603-1

CRITICAL U9340 74LVC2G132 US8

10MS RC GENERATES ONE-SHOT LOW PULSE ON INT0# TO ALLOW PART TO WAKE UP AND XTAL TO START

SST8051 C9390 22PF 5% 25V NP0-C0G 201

SST8051 C9391 22PF 5% 25V NP0-C0G 201

OMIT Y9390 14.318MHZ-35PPF-20PF SM-2.5X2.0MM

=PP3V3_S0_HDCP

SST8051 C9326 0.1UF 10% 6.3V X5R 201

CRITICAL U9325 TC7SH00FEF SON

TMDS_HW_RESET_L

SST8051_SW_RESET_L

SST8051 R9325 10K 1% 1/20W MF 201

SST8051 CRITICAL L9300 FERR-120-OHM-1.5A 0402-LF

PP3V3_S0_HDCP_F

SST8051 C9302 0.01UF 10% 10V X5R 201

SST8051 C9301 0.1UF 10% 6.3V X5R 201

SST8051 CRITICAL C9300 10UF 20% 6.3V X5R 603

CRITICAL U9300 SST89V54RD WQFN

DVI_HOTPLUG_DET_INT_L	7	(INT0#)P3.2	
TMDS_LINT_L	8	(INT1#)P3.3	
TP_SST8051_RXD	5	(RXD)P3.0	
SST8051_P34_AUDIO_CONFIG	9	(T0)P3.4	
NC	10	(T1)P3.5	
NC	12	(RD#)P3.7	
NC	11	(WR#)P3.6	
TP_SST8051_TXD	6	(TXD)P3.1	
SST8051_XTAL1	14	XTAL1	
SST8051_XTAL2	13	XTAL2	
SST8051_RST	4	RST	
SST8051_EA_L	26	EA*	
NC	25	ALE/PROG*	
SST8051_PSEN_L	24	PSEN*	
THRM_PAD	41		
VSS	15		
P0.0(AD0)	34		
P0.1(AD1)	33		
P0.2(AD2)	32		
P0.3(AD3)	31		
P0.4(AD4)	30	NC	
P0.5(AD5)	29		
P0.6(AD6)	28		
P0.7(AD7)	27		
P1.0(T2)	36	SST8051_PSEN_L	
P1.1(T2_EX)	37	DVI_HOTPLUG_DET_BUF	
P1.2(ECI)	38	SST8051_DVI_HOTPLUG_DET	
P1.3(CEX0)	39	NC	
P1.4(CEX1/SS*)	40	SST8051_DDC_CLK	
(CEX2/MOSI)P1.5	1	SST8051_DDC_DATA	
(CEX3/MISO)P1.6	2		
(CEX4/SCK)P1.7	3		
A8(P2.0)	16	NC	
A9(P2.1)	17	NC	
A10(P2.2)	18	NC	
A11(P2.3)	19	NC	
A12(P2.4)	20	NC	
P2.5(A13)	21	SST8051_P25_AUDIO_CONFIG	
P2.6(A14)	22	NC	
P2.7(A15)	23	NC	

=PP3V3_S0_HDCP

SST8051 R9302 2.2K 5% 1/20W MF 201

SST8051 R9303 2.2K 5% 1/20W MF 201

SST8051 R9304 2.2K 5% 1/20W MF 201

SST8051 R9305 2.2K 5% 1/20W MF 201

SST8051 R9306 4.7K 5% 1/20W MF 201

SST8051_DDC_EN

TMDS_DDC_SCL

SST8051 Q9300 SSM6N15FE SOT563

TMDS_DDC_SDA

SST8051 Q9300 SSM6N15FE SOT563

TMDS_LSCL

TMDS_LSDA

NO STUFF
SST8051_DVI_HOTPLUG_DET — R9350 0 5% 1/20W MF 201 — DVI_HOTPLUG_DET

DVI_HOTPLUG_DET_BUF — R9351 0 5% 1/20W MF 201

STUFFING OPTION CHOOSES RAW OR CONTROLLER OUTPUT OF DVI_HOTPLUG_DET

SST8051_UPDATE_L — SST8051_PSEN_L
MAKE_BASE=TRUE

SST8051_UPDATE_L pulled up to 10K at SB

=PP3V3_S0_HDCP

SST8051 R9330 4.7K 1% 1/20W MF 201

SST8051_P25_AUDIO_CONFIG

AUDIO CONFIG OPTIONS

P25	P34	OPTION
0	0	HD AUDIO
0	1	SPDIF
1	0	NO AUDIO
1	1	RESERVED

=PP3V3_S0_HDCP

SST8051 R9301 10K 1% 1/20W MF 201

SST8051_EA_L

SST8051_P34_AUDIO_CONFIG

SST8051 R9333 4.7K 1% 1/20W MF 201

HDCP uController

SYNC_MASTER= SYNC_DATE=

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Video Connectors

TMDS(MICRO DVI) INTERFACE
EXTERNAL VIDEO (VGA) INTERFACE

NB VIDEO ALIASES

=CRT_TVO_IREF = CRT_TVO_IREF
=TV_A_DAC = TV_A_DAC
=TV_B_DAC = TV_B_DAC
=TV_C_DAC = TV_C_DAC
=CRT_BLUE = CRT_BLUE
=CRT_GREEN = CRT_GREEN
=CRT_RED = CRT_RED
=CRT_HSYNC_R = CRT_HSYNC_R
=CRT_VSYNC_R = CRT_VSYNC_R
(MAKE_BASE=TRUE)

Isolation required for DVI power switch

A 1.3K OHM 1% RESISTOR IS REQUIRED BETWEEN CRT_IREF AND GROUND

R9469 1.3K 1% 1/20W MF 201 — CRT_TVO_IREF

CRITICAL F9404 0.5AMP-13.2V SM-LF
=PP5V_S0_TMDS (VOLTAGE=5V, MIN_LINE_WIDTH=0.30 MM, MIN_NECK_WIDTH=0.20 MM) → PP5V_S0_TMDS_FUSE (VOLTAGE=5V, MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM)
L9444 600-OHM-300MA 0402
PP5V_S0_DVIPORT (VOLTAGE=5V, MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.25 MM)
C9404 0.1UF 10% 16V X5R 402

=PP3V3_S0_NB
R9466 2.2K 5% 1/20W MF 201 — TV_DCONSEL<0>
R9467 2.2K 5% 1/20W MF 201 — TV_DCONSEL<1>

D9401 1SS418 SOD-723
PP5V_S0_DVIPORT_D (VOLTAGE=5V, MIN_LINE_WIDTH=0.2 MM, MIN_NECK_WIDTH=0.2 MM)

R9462 1K 5% 1/20W MF 201
R9463 1K 5% 1/20W MF 201

=PP3V3_S0_TMDS — R9480 10K 5% 1/20W MF 201 — DVI_HOST
HDMI_HOST — R9481 100K 5% 1/20W MF 201

TMDS_HTPLG
C9410 1000PF 10% 16V X7R 201
TMDS_DDC_SDA
NOSTUFF C9411 100PF 5% 25V CERM 201
TMDS_DDC_SCL
NOSTUFF C9412 100PF 5% 25V CERM 201

SB_CRT_TVOUT_MUX_L

PLACE R9450 R9451 CLOSE TO NB
TV_A_DAC, CRT_BLUE
R9450 150 1% 1/20W MF 201 — =TV_A_RTN (VOLTAGE=0V)
R9451 150 1% 1/20W MF 201 — =CRT_BLUE_L (VOLTAGE=0V)

PLACE U9401 NEAR NB
=PP3V3_S0_NB
C9439 0.1UF 10% 16V X5R 201
U9401 FSAV430 DQFN (CRITICAL)
S, 1B1, 1B2, 1A, 2B1, 2B2, 2A, OE*, 4B1, 4B2, 4A, 3B1, 3B2, 3A, NC, GND, THMPAD

PLACE R9452 R9453 CLOSE TO NB
TV_B_DAC, CRT_GREEN
R9452 150 1% 1/20W MF 201 — =TV_B_RTN (VOLTAGE=0V)
R9453 150 1% 1/20W MF 201 — =CRT_GREEN_L (VOLTAGE=0V)

PLACE R9454 R9455 CLOSE TO NB
TV_C_DAC, CRT_RED
R9454 150 1% 1/20W MF 201 — =TV_C_RTN (VOLTAGE=0V)
R9455 150 1% 1/20W MF 201 — =CRT_RED_L (VOLTAGE=0V)

EXT_C_R, EXT_Y_G, EXT_COMPVID_B
FL9400 210MHZ MEA2010P-SM (CRITICAL)
VGA_B, VGA_G, VGA_R

These nets connect to RIO connector J4200:
TMDS_TX_CONN_P<2>, TMDS_TX_CONN_N<2>, TMDS_TX_CONN_P<1>, TMDS_TX_CONN_N<1>, TMDS_TX_CONN_P<0>, TMDS_TX_CONN_N<0>, TMDS_TX_CONN_CLK_P, TMDS_TX_CONN_CLK_N

PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR CONNECTOR

=PP3V3_S0_TMDS — C9460 0.1UF 10% 6.3V X5R 201
CRITICAL U9404 SN74LVC2G125DCU (VCC, GND)
CRT_HSYNC_R — R9460 39 5% 1/20W MF 201 — CRT_HSYNC_LS_R — 125 — CRT_HSYNC_LS — R9470 39 5% 1/20W MF 201 — VGA_HSYNC
NOSTUFF C9442 33PF 5% 25V NP0-C0G 201

PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR THE CONNECTOR

CRITICAL U9404 SN74LVC2G125DCU (VCC, GND)
CRT_VSYNC_R — R9461 39 5% 1/20W MF 201 — CRT_VSYNC_LS_R — 125 — CRT_VSYNC_LS — R9471 39 5% 1/20W MF 201 — VGA_VSYNC
NOSTUFF C9443 33PF 5% 25V NP0-C0G 201

CRITICAL L9405 90-OHM-100MA 1210-4SM1 — TMDS_TX_P<2>, TMDS_TX_N<2>
CRITICAL L9407 90-OHM-100MA 1210-4SM1 — TMDS_TX_P<1>, TMDS_TX_N<1>
CRITICAL L9406 90-OHM-100MA 1210-4SM1 — TMDS_TX_P<0>, TMDS_TX_N<0>
CRITICAL L9404 300-OHM-100MA 1210-4SM1 — TMDS_TX_CLK_P, TMDS_TX_CLK_N

Place components near J4200 unless otherwise noted

DVI CONNECTIONS

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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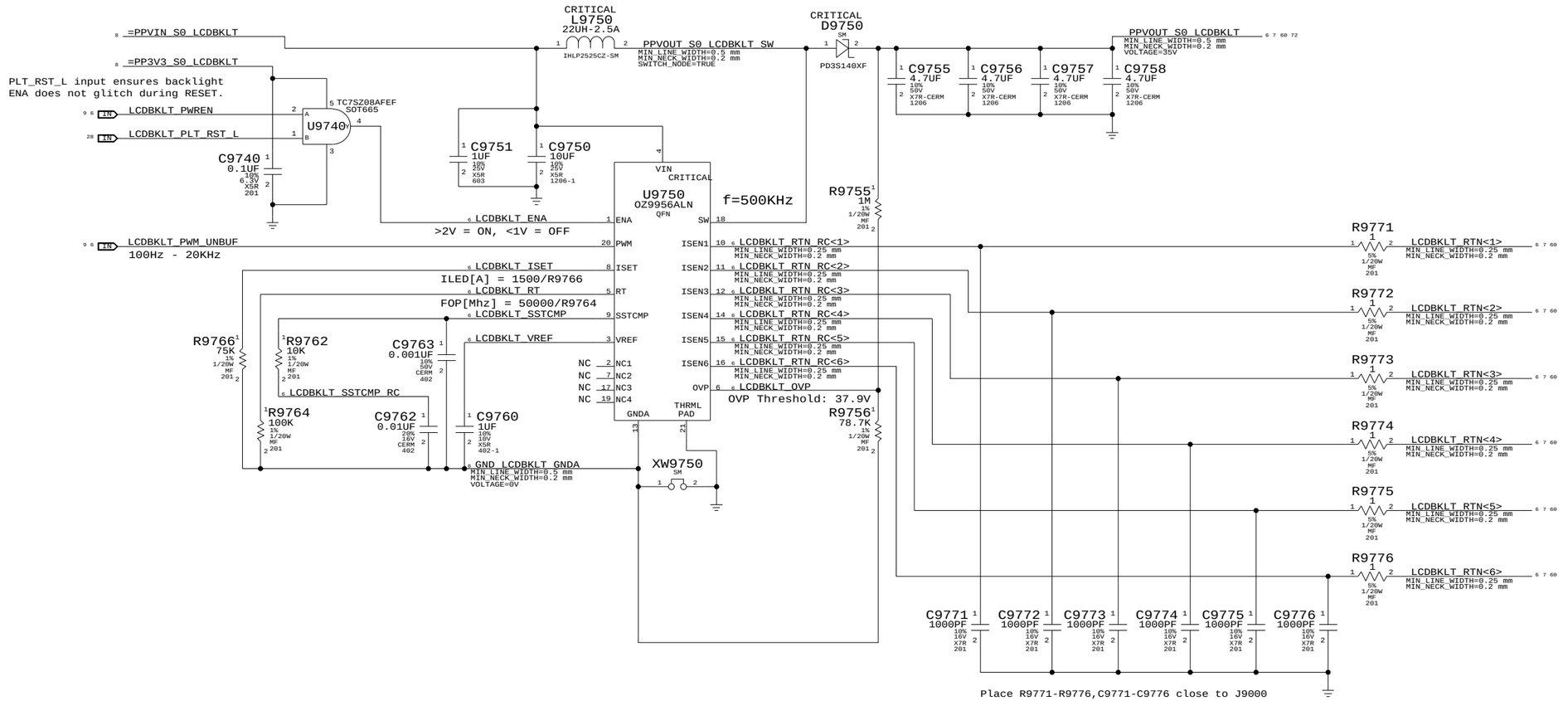
LED Backlight Driver



LED Backlight Driver

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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ADDITIONAL CPU VCORE HF DECOUPLING

40x 1uF 0402

12 11 8 =PPVCORE_S0_CPU

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C9900 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9901 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9902 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9903 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9904 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9905 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9906 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9907 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9908 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9909 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C9910 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9911 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9912 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9913 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9914 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9915 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9916 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9917 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9918 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9919 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C9920 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9921 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9922 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9923 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9924 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9925 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9926 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9927 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9928 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9929 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C9930 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9931 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9932 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9933 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9934 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9935 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9936 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9937 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9938 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9939 2.2UF 20% 6.3V CERM 402-LF

ADDITIONAL GPU VCORE HF DECOUPLING

18x 1uF 0402

53 22 18 8 =PPVCORE_S0_NB_GFX

OMIT 1 C9980 2 2.2UF 20% 6.3V CERM 402-LF	OMIT 1 C9981 2 2.2UF 20% 6.3V CERM 402-LF	OMIT 1 C9982 2 2.2UF 20% 6.3V CERM 402-LF	OMIT 1 C9983 2 2.2UF 20% 6.3V CERM 402-LF	OMIT 1 C9984 2 2.2UF 20% 6.3V CERM 402-LF	OMIT 1 C9985 2 2.2UF 20% 6.3V CERM 402-LF	OMIT 1 C9986 2 2.2UF 20% 6.3V CERM 402-LF	OMIT 1 C9987 2 2.2UF 20% 6.3V CERM 402-LF	OMIT 1 C9988 2 2.2UF 20% 6.3V CERM 402-LF	OMIT 1 C9989 2 2.2UF 20% 6.3V CERM 402-LF

OMIT 1 C9990 2 2.2UF 20% 6.3V CERM 402-LF	OMIT 1 C9991 2 2.2UF 20% 6.3V CERM 402-LF	OMIT 1 C9992 2 2.2UF 20% 6.3V CERM 402-LF	OMIT 1 C9993 2 2.2UF 20% 6.3V CERM 402-LF	OMIT 1 C9994 2 2.2UF 20% 6.3V CERM 402-LF	OMIT 1 C9995 2 2.2UF 20% 6.3V CERM 402-LF	OMIT 1 C9996 2 2.2UF 20% 6.3V CERM 402-LF	OMIT 1 C9997 2 2.2UF 20% 6.3V CERM 402-LF

Additional CPU/GPU Decoupling

SYNC_MASTER= SYNC_DATE=

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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	ISL3,ISL10	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_4MIL	*	0.100 MM	?
FSB_9MIL	*	0.228 MM	?
FSB_DATA	*	=FSB_4MIL	?
FSB_DATA2DATA	*	=FSB_4MIL	?
FSB_DSTB	*	=FSB_9MIL	?
FSB_DATA2DSTB	*	=FSB_9MIL	?
FSB_ADDR	*	=FSB_4MIL	?
FSB_ADDR2ADDR	*	=FSB_4MIL	?
FSB_ADSTB	*	=FSB_9MIL	?
FSB_ADDR2ADSTB	*	=FSB_9MIL	?
FSB_COMMON	*	=FSB_4MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_70D	*	Y	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2TO1	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?
CPU_THERMD	*	25 MIL	?

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance.

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

CPU / FSB Net Properties

NET_TYPE ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_ADS_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BNR_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BPRI_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BREQ0_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DBSY_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DEFER_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DPWR_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DRDY_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_HIT_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_HITM_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_LOCK_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_TRDY_L	10 14
FSB_CPURST_L	FSB_55S	FSB_COMMON	FSB_CPURST_L	6 10 13 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_D_L<15..0>	10 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_DINV_L<0>	10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<0>	10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<0>	10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_D_L<31..16>	10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_DINV_L<1>	10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<1>	10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<1>	10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_D_L<47..32>	10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_DINV_L<2>	10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<2>	10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<2>	10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_D_L<63..48>	10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_DINV_L<3>	10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<3>	10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<3>	10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_A_L<16..3>	10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	10 14
FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<0>	10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB_A_L<35..17>	10 14
FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<1>	10 14
CPU_IERR_L	CPU_55S		CPU_IERR_L	6 10
CPU_FERR_L	CPU_55S		CPU_FERR_L	6 10 23
CPU_PROCHOT_L	CPU_55S	CPU_2TO1	CPU_PROCHOT_L	6 10 42 52
CPU_PWRGD	CPU_55S		CPU_PWRGD	6 10 13 23
CPU_FROM_SB	CPU_55S		CPU_INTR	6 10 23
CPU_FROM_SB	CPU_55S		CPU_NMI	6 10 23
CPU_FROM_SB	CPU_55S		CPU_A20M_L	6 10 23
CPU_FROM_SB	CPU_55S		CPU_DPSLP_L	6 10 23
CPU_FROM_SB	CPU_55S		CPU_IGNNE_L	6 10 23
CPU_INIT_L	CPU_55S		CPU_INIT_L	6 10 23
CPU_FROM_SB	CPU_55S		CPU_SMI_L	6 10 23
CPU_FROM_SB	CPU_55S		CPU_STPCLK_L	6 10 23
PM_THRMTRIP_L	CPU_55S	CPU_2TO1	PM_THRMTRIP_L	6 10 16 23 42
FSB_CPUSLP_L	CPU_55S		FSB_CPUSLP_L	10 14
PM_DPRSLPVR	CPU_55S	CPU_2TO1	PM_DPRSLPVR	6 16 25 52
(See above)	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	6 52
CPU_BSEL0	CPU_55S	CPU_2TO1	CPU_BSEL<0>	6 10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<0>	6 7 13 16 30
CPU_BSEL1	CPU_55S	CPU_2TO1	CPU_BSEL<1>	6 10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<1>	6 7 13 16 30
CPU_BSEL2	CPU_55S	CPU_2TO1	CPU_BSEL<2>	6 10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<2>	6 7 13 16 30
CPU_DPRSTP_L	CPU_55S	CPU_2TO1	CPU_DPRSTP_L	6 10 16 23 52
CPU_GTLREF	CPU_55S	CPU_GTLREF	CPU_GTLREF	6 10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<3>	6 10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	6 10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<1>	6 10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	6 10
XDP_TDI	CPU_55S	CPU_ITP	XDP_TDI	6 7 10 13
XDP_TDO	CPU_55S	CPU_ITP	XDP_TDO	6 7 10 13
XDP_TMS	CPU_55S	CPU_ITP	XDP_TMS	6 7 10 13
XDP_TCK	CPU_55S	CPU_ITP	XDP_TCK	6 7 10 13
XDP_TRST_L	CPU_55S	CPU_ITP	XDP_TRST_L	6 7 10 13
XDP_BPM_L	CPU_55S	CPU_ITP	XDP_BPM_L<4..0>	6 7 10 13
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP_BPM_L<5>	6 7 10 13
	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	6 7 13 30 71
	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	6 7 13 30 71
(FSB_CPURST_L)	CPU_55S	CPU_ITP	XDP_CPURST_L	6 7 13
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	6 11 12 52
	CPU_55S	CPU_2TO1	IMVP6_VID<6..0>	12
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	6 11 52
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	6 11 52
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	6 52
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	6 52
	CPU_70D	CPU_THERMD	CPU_THERMD_P	6 10 46
	CPU_70D	CPU_THERMD	CPU_THERMD_N	6 10 46

CPU/FSB Constraints

SYNC_MASTER=T9 SYNC_DATE=01/30/2007

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D	051-7230	J
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PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
PCIE_R2D_2_PCIE_R2D	*	0.228 MM	?
PCIE_D2R_2_PCIE_D2R	*	0.228 MM	?
PCIE_R2D_2_PCIE_D2R	*	0.300 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_N2S_2_DMI_N2S	*	0.228 MM	?
DMI_S2N_2_DMI_S2N	*	0.228 MM	?
DMI_N2S_2_DMI_S2N	*	0.300 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_R2D	PCIE_R2D	*	PCIE_R2D_2_PCIE_R2D
PCIE_D2R	PCIE_D2R	*	PCIE_D2R_2_PCIE_D2R
PCIE_R2D	PCIE_D2R	*	PCIE_R2D_2_PCIE_D2R

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_N2S	DMI_N2S	*	DMI_N2S_2_DMI_N2S
DMI_S2N	DMI_S2N	*	DMI_S2N_2_DMI_S2N
DMI_N2S	DMI_S2N	*	DMI_N2S_2_DMI_S2N

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_R2D	PWR	*	BUS2PWR_GND
PCIE_R2D	GND	*	BUS2PWR_GND
PCIE_D2R	PWR	*	BUS2PWR_GND
PCIE_D2R	GND	*	BUS2PWR_GND
DMI_N2S	PWR	*	BUS2PWR_GND
DMI_N2S	GND	*	BUS2PWR_GND
DMI_S2N	PWR	*	BUS2PWR_GND
DMI_S2N	GND	*	BUS2PWR_GND
LVDS	PWR	*	BUS2PWR_GND
LVDS	GND	*	BUS2PWR_GND
TMDS	PWR	*	BUS2PWR_GND
TMDS	GND	*	BUS2PWR_GND

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CRT_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TMDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS	*	20 MIL	?
CRT	*	25 MIL	?
CRT_2CRT	*	20 MIL	?
CRT_SYNC	*	25 MIL	?
CRT_SYNC2SYNC	*	20 MIL	?
TVDAC	*	25 MIL	?
TVDAC_2TVDAC	*	20 MIL	?
LVDS2LVDS	*	0.300 MM	?
TMDS	*	20 MIL	?

DG Says 40 mil spacing minimum

DG Says 30 mil spacing minimum

DG Says 40 mil spacing minimum

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT
CRT_SYNC	CRT_SYNC	*	CRT_SYNC2SYNC
TVDAC	TVDAC	*	TVDAC_2TVDAC
LVDS	LVDS	*	LVDS2LVDS

LVDS signals are 100-ohm +/- 20% differential impedence.
CRT & TVDAC signal single-ended impedence varies by location:
- 37.5-ohm +/- 15% from GMCH to first termination resistor.
- 50-ohm +/- 15% from first to second termination resistor.
- 55-ohm +/- 15% from second termination resistor to connector.

CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedence.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PEG_R2D	PCIE_100D	PCIE_R2D	PEG_R2D_P<15..0>	
	PCIE_100D	PCIE_R2D	PEG_R2D_N<15..0>	
	PCIE_100D	PCIE_R2D	PEG_R2D_C_P<15..0>	6 9 15 61
	PCIE_100D	PCIE_R2D	PEG_R2D_C_N<15..0>	6 9 15 61
PEG_D2R	PCIE_100D	PCIE_D2R	PEG_D2R_P<15..0>	6 9 15 61
	PCIE_100D	PCIE_D2R	PEG_D2R_N<15..0>	6 9 15 61
	PCIE_100D	PCIE_D2R	PEG_D2R_C_P<15..0>	
	PCIE_100D	PCIE_D2R	PEG_D2R_C_N<15..0>	
DMI_N2S	DMI_100D	DMI_N2S	DMI_N2S_P<3..0>	6 16 24
	DMI_100D	DMI_N2S	DMI_N2S_N<3..0>	6 16 24
DMI_S2N	DMI_100D	DMI_S2N	DMI_S2N_P<3..0>	6 16 24
	DMI_100D	DMI_S2N	DMI_S2N_N<3..0>	6 16 24
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_P	6 15 60
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_N	6 15 60
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_P<2..0>	6 7 15 60
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_N<2..0>	6 7 15 60
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_F_P<2..0>	6 60
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_F_N<2..0>	6 60
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS_A_DATA_P<3>	9
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS_A_DATA_N<3>	9
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_P	9 15
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_N	9 15
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_P<2..0>	9 15
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_N<2..0>	9 15
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS_B_DATA_P<3>	9
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS_B_DATA_N<3>	9
LVDS_IBG		LVDS	LVDS_IBG	6 15 60
CRT_TVO_IREF		CRT	CRT_TVO_IREF	6 63
CRT_RED	CRT_50S	CRT	CRT_RED	6 63
CRT_GREEN	CRT_50S	CRT	CRT_GREEN	6 63
CRT_BLUE	CRT_50S	CRT	CRT_BLUE	6 63
CRT_SYNC	CRT_55S	CRT_SYNC	CRT_HSYNC_R	6 63
CRT_SYNC	CRT_55S	CRT_SYNC	CRT_VSYNC_R	6 63
TV_A_DAC	CRT_50S	TVDAC	TV_A_DAC	6 63
TV_B_DAC	CRT_50S	TVDAC	TV_B_DAC	6 63
TV_C_DAC	CRT_50S	TVDAC	TV_C_DAC	6 63
EXT_COMPVID_B	CRT_50S	CRT	EXT_COMPVID_B	6 63
EXT_Y_G	CRT_50S	CRT	EXT_Y_G	6 63
EXT_C_R	CRT_50S	CRT	EXT_C_R	6 63
VGA_R	CRT_50S	CRT	VGA_R	6 7 37 63
VGA_G	CRT_50S	CRT	VGA_G	6 7 37 63
VGA_B	CRT_50S	CRT	VGA_B	6 7 37 63
	PCIE_100D	PCIE_R2D	TMDS_SDB_P	6 61
	PCIE_100D	PCIE_R2D	TMDS_SDB_N	6 61
	PCIE_100D	PCIE_R2D	TMDS_SDC_P	6 61
	PCIE_100D	PCIE_R2D	TMDS_SDC_N	6 61
	PCIE_100D	PCIE_R2D	TMDS_SDG_P	6 61
	PCIE_100D	PCIE_R2D	TMDS_SDG_N	6 61
	PCIE_100D	PCIE_R2D	TMDS_SDR_P	6 61
	PCIE_100D	PCIE_R2D	TMDS_SDR_N	6 61
	TMDS_100D	TMDS	TMDS_TX_CLK_P	6 61 63
	TMDS_100D	TMDS	TMDS_TX_CLK_N	6 61 63
	PCIE_100D	PCIE_D2R	TMDS_INT_P	6 61
	PCIE_100D	PCIE_D2R	TMDS_INT_N	6 61
	TMDS_100D	TMDS	TMDS_TX_CONN_CLK_P	6 7 37 63
	TMDS_100D	TMDS	TMDS_TX_CONN_CLK_N	6 7 37 63
	TMDS_100D	TMDS	TMDS_CONN_P<3..0>	
	TMDS_100D	TMDS	TMDS_CONN_N<3..0>	
	TMDS_100D	TMDS	TMDS_TX_P<3..0>	6 61 63
	TMDS_100D	TMDS	TMDS_TX_N<3..0>	6 61 63
	SMB_55S	SMB	TMDS_DDC_SCL	6 7 37 61 62 63
	SMB_55S	SMB	TMDS_DDC_SDA	6 7 37 61 62 63

NB Constraints

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SIZE	DRAWING NUMBER	REV.
D	051-7230	J

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DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	ISL3,ISL10	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_87D	*	=87_OHM_DIFF	=87_OHM_DIFF	=87_OHM_DIFF	=87_OHM_DIFF	=87_OHM_DIFF	=87_OHM_DIFF
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=2.28:1_SPACING	?
MEM_CTRL2CTRL	*	=1:1_SPACING	?
MEM_CTRL2MEM	*	=2.28:1_SPACING	?
MEM_CMD2CMD	*	=1:1_SPACING	?
MEM_CMD2MEM	*	=2.28:1_SPACING	?
MEM_DATA2DATA	*	=1:1_SPACING	?
MEM_DATA2MEM	*	=2.28:1_SPACING	?
MEM_DQS2MEM	*	=2.28:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PP1V8_MEM	*	PWR_P2MM
MEM_CTRL	PP1V8_MEM	*	PWR_P2MM
MEM_DATA	PP1V8_MEM	*	PWR_P2MM
MEM_DQS	PP1V8_MEM	*	PWR_P2MM
MEM_CMD	PP1V8_MEM	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	NB_STATIC	*	PWR_P2MM
MEM_CTRL	NB_STATIC	*	PWR_P2MM
MEM_DATA	NB_STATIC	*	PWR_P2MM
MEM_DQS	NB_STATIC	*	PWR_P2MM
MEM_CMD	NB_STATIC	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

Need to support MEM_*-style wildcards!

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	PWR	*	BUS2PWR_GND
MEM_CLK	GND	*	BUS2PWR_GND
MEM_CTRL	PWR	*	BUS2PWR_GND
MEM_CTRL	GND	*	BUS2PWR_GND
MEM_CMD	PWR	*	BUS2PWR_GND
MEM_CMD	GND	*	BUS2PWR_GND
MEM_DATA	PWR	*	BUS2PWR_GND
MEM_DATA	GND	*	BUS2PWR_GND
MEM_DQS	PWR	*	BUS2PWR_GND
MEM_DQS	GND	*	BUS2PWR_GND

I93	PP0V9_S3M_MEM_NBVREFB	NET_SPACING_TYPE=NB_STATIC 8 16 21
I95	PP0V9_S3M_MEM_NBVREFA	NET_SPACING_TYPE=NB_STATIC 8 16 21
I94	NB_VCCSM_LF1	NET_SPACING_TYPE=NB_STATIC 6 18
I96	NB_VCCSM_LF2	NET_SPACING_TYPE=NB_STATIC 6 18
I97	NB_VCCSM_LF3	NET_SPACING_TYPE=NB_STATIC 6 18
I98	NB_VCCSM_LF4	NET_SPACING_TYPE=NB_STATIC 6 18
I99	NB_VCCSM_LF5	NET_SPACING_TYPE=NB_STATIC 6 18
I101	NB_VCCSM_LF6	NET_SPACING_TYPE=NB_STATIC 6 18
I610	NB_VCCSM_LF7	NET_SPACING_TYPE=NB_STATIC 6 18
I102	=PP1V8_S3M_MEM_NB	NET_SPACING_TYPE=PP1V8_MEM 8 16 18 21
	GND	NET_SPACING_TYPE=GND

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	MEM_87D	MEM_CLK	MEM_CLK_P<2..0> 16 31 33
	MEM_87D	MEM_CLK	MEM_CLK_N<2..0> 16 31 33
	MEM_45S	MEM_CTRL	MEM_CKE<1..0> 16 31 33
	MEM_45S	MEM_CTRL	MEM_CS_L<1..0> 16 31 33
	MEM_45S	MEM_CTRL	MEM_ODT<1..0> 6 16 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_A<13..0> 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_BS<2..0> 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_RAS_L 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_CAS_L 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_WE_L 17 31 33
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_A_DQ<7..0> 17 31
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A_DQ<15..8> 17 31
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_A_DQ<23..16> 17 31
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A_DQ<31..24> 17 31
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_A_DQ<39..32> 17 31
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_A_DQ<47..40> 17 31
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A_DQ<55..48> 17 31
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A_DQ<63..56> 17 31
MEM_A_DM0	MEM_55S	MEM_DATA	MEM_A_DM<0> 17 31
MEM_A_DM1	MEM_55S	MEM_DATA	MEM_A_DM<1> 17 31
MEM_A_DM2	MEM_55S	MEM_DATA	MEM_A_DM<2> 17 31
MEM_A_DM3	MEM_55S	MEM_DATA	MEM_A_DM<3> 17 31
MEM_A_DM4	MEM_55S	MEM_DATA	MEM_A_DM<4> 17 31
MEM_A_DM5	MEM_55S	MEM_DATA	MEM_A_DM<5> 17 31
MEM_A_DM6	MEM_55S	MEM_DATA	MEM_A_DM<6> 17 31
MEM_A_DM7	MEM_55S	MEM_DATA	MEM_A_DM<7> 17 31
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0> 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<0> 17 31
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1> 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<1> 17 31
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2> 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<2> 17 31
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3> 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<3> 17 31
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4> 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<4> 17 31
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5> 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<5> 17 31
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6> 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<6> 17 31
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7> 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<7> 17 31
	MEM_87D	MEM_CLK	MEM_CLK_P<5..3> 16 32 33
	MEM_87D	MEM_CLK	MEM_CLK_N<5..3> 16 32 33
	MEM_45S	MEM_CTRL	MEM_CKE<4..3> 16 32 33
	MEM_45S	MEM_CTRL	MEM_CS_L<3..2> 16 32 33
	MEM_45S	MEM_CTRL	MEM_ODT<3..2> 6 16 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_A<13..0> 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_BS<2..0> 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_RAS_L 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_CAS_L 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_WE_L 17 32 33
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B_DQ<7..0> 17 32
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_B_DQ<15..8> 17 32
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_B_DQ<23..16> 17 32
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B_DQ<31..24> 17 32
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B_DQ<39..32> 17 32
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B_DQ<47..40> 17 32
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_B_DQ<55..48> 17 32
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B_DQ<63..56> 17 32
MEM_B_DM0	MEM_55S	MEM_DATA	MEM_B_DM<0> 17 32
MEM_B_DM1	MEM_55S	MEM_DATA	MEM_B_DM<1> 17 32
MEM_B_DM2	MEM_55S	MEM_DATA	MEM_B_DM<2> 17 32
MEM_B_DM3	MEM_55S	MEM_DATA	MEM_B_DM<3> 17 32
MEM_B_DM4	MEM_55S	MEM_DATA	MEM_B_DM<4> 17 32
MEM_B_DM5	MEM_55S	MEM_DATA	MEM_B_DM<5> 17 32
MEM_B_DM6	MEM_55S	MEM_DATA	MEM_B_DM<6> 17 32
MEM_B_DM7	MEM_55S	MEM_DATA	MEM_B_DM<7> 17 32
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0> 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<0> 17 32
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1> 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<1> 17 32
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2> 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<2> 17 32
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3> 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<3> 17 32
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4> 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<4> 17 32
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5> 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<5> 17 32
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6> 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<6> 17 32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7> 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<7> 17 32

Memory Constraints

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Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_60S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	20 MIL	?
USB_2CLK	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	PWR	*	BUS2PWR_GND
USB	GND	*	BUS2PWR_GND

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
IDE_PDD	IDE_55S	IDE	IDE_PDD<15..0> 6 23 38
IDE_PDA	IDE_55S	IDE	IDE_PDA<2..0> 6 23 38
IDE_PDCS	IDE_55S	IDE	IDE_PDCS1_L 6 23 38
IDE_PDCS	IDE_55S	IDE	IDE_PDCS3_L 6 23 38
IDE_CNTL	IDE_55S	IDE	IDE_PDIOW_L 6 23 38
IDE_PDIOR_L	IDE_55S	IDE	IDE_PDIOR_L 6 23 38
IDE_CNTL	IDE_55S	IDE	IDE_PDDACK_L 6 23 38
IDE_CNTL	IDE_55S	IDE	IDE_PDDREQ 6 23 38
IDE_PDIORDY	IDE_55S	IDE	IDE_PDIORDY 6 23 38
IDE_IRQ14	IDE_55S	IDE	IDE_IRQ14 6 23 38
IDE_RST_L	IDE_55S	IDE	ODD_RST_5VTOL_L
SATA_A_R2D	SATA_100D	SATA	SATA_A_R2D_C_P 9 23
	SATA_100D	SATA	SATA_A_R2D_C_N 9 23
	SATA_100D	SATA	SATA_A_R2D_P
	SATA_100D	SATA	SATA_A_R2D_N
SATA_A_D2R	SATA_100D	GND	SATA_A_D2R_P 9
	SATA_100D	GND	SATA_A_D2R_N 9
	SATA_100D	SATA	SATA_A_D2R_C_P
	SATA_100D	SATA	SATA_A_D2R_C_N
SATA_B_R2D	SATA_100D	SATA	SATA_B_R2D_C_P 9 23
	SATA_100D	SATA	SATA_B_R2D_C_N 9 23
	SATA_100D	SATA	SATA_B_R2D_P
	SATA_100D	SATA	SATA_B_R2D_N
SATA_A_D2R	SATA_100D	GND	SATA_B_D2R_P 9
	SATA_100D	GND	SATA_B_D2R_N 9
	SATA_100D	SATA	SATA_B_D2R_C_P
	SATA_100D	SATA	SATA_B_D2R_C_N
SATA_C_R2D	SATA_100D	SATA	SATA_C_R2D_C_P 9 23
	SATA_100D	SATA	SATA_C_R2D_C_N 9 23
	SATA_100D	SATA	SATA_C_R2D_P
	SATA_100D	SATA	SATA_C_R2D_N
SATA_A_D2R	SATA_100D	GND	SATA_C_D2R_P 9
	SATA_100D	GND	SATA_C_D2R_N 9
	SATA_100D	SATA	SATA_C_D2R_C_P
	SATA_100D	SATA	SATA_C_D2R_C_N
SATA_RBIAS	SATA_55S		SATA_RBIAS
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK 6 9 23
	HDA_55S	HDA	HDA_BIT_CLK_R 6 23
HDA_SYNC	HDA_55S	HDA	HDA_SYNC 6 7 9 23 37
	HDA_55S	HDA	HDA_SYNC_R 6 23
HDA_RST_L	HDA_55S	HDA	HDA_RST_L 6 9 23 37
	HDA_55S	HDA	HDA_RST_L_R 6 23
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0 6 9 23
	HDA_55S	HDA	HDA_SDIN_CODEC
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT 6 9 23
	HDA_55S	HDA	HDA_SDOUT_R 6 23
USB_EXTA	USB_90D	USB	USB_EXTA_P 9 24
	USB_90D	USB	USB_EXTA_N 9 24
	USB_90D	USB	USB_EXTA_MUXED_P 9
	USB_90D	USB	USB_EXTA_MUXED_N 9
USB_MINI	USB_90D	USB	USB_MINI_P 9 24
	USB_90D	USB	USB_MINI_N 9 24
USB_EXTD	USB_90D	USB	USB_EXTD_P 9 24
	USB_90D	USB	USB_EXTD_N 9 24
USB_CAMERA	USB_90D	USB	USB_CAMERA_P 9 24
	USB_90D	USB	USB_CAMERA_N 9 24
USB_BT	USB_90D	USB	USB_BT_P 9 24
	USB_90D	USB	USB_BT_N 9 24
USB_TPAD	USB_90D	USB	USB_TPAD_P 9 24
	USB_90D	USB	USB_TPAD_N 9 24
USB_IR	USB_90D	USB	USB_IR_P 6 9 24
	USB_90D	USB	USB_IR_N 6 9 24
USB_EXTB	USB_90D	USB	USB_EXTB_P 9 24
	USB_90D	USB	USB_EXTB_N 9 24
USB_EXCARD	USB_90D	USB	USB_EXCARD_P 9 24
	USB_90D	USB	USB_EXCARD_N 9 24
USB_EXTC	USB_90D	USB	USB_EXTC_P 9 24
	USB_90D	USB	USB_EXTC_N 9 24
	USB_90D	USB	USB2_AIRPORT_P_F 6 36
	USB_90D	USB	USB2_AIRPORT_N_F 6 36
	USB_90D	USB	USB2_CAMERA_F_P 6 7 60
	USB_90D	USB	USB2_CAMERA_F_N 6 7 60
	USB_90D	USB	USB2_EXTA_F_P 6 7 37 39
	USB_90D	USB	USB2_EXTA_F_N 6 7 37 39
			USB2_3G_F_P
			USB2_3G_F_N
USB_RBIAS	USB_60S		USB_RBIAS 6 24
SMB_SB_SCL	SMB_55S	SMB	SMB_CLK 25 44
SMB_SB_SDA	SMB_55S	SMB	SMB_DATA 25 44
SMB_SB_ME_SCL	SMB_55S	SMB	SMB_ME_CLK 25 44
SMB_SB_ME_SDA	SMB_55S	SMB	SMB_ME_DATA 25 44
SPI_SCLK	SPI_55S	SPI	SPI_SCLK_R 6 24 49
	SPI_55S	SPI	SPI_SCLK
	SPI_55S	SPI	SPI_A_SCLK_R 6 43 49
	SPI_55S	SPI	SPI_B_SCLK_R
SPI_SI	SPI_55S	SPI	SPI_SI_R 6 24 49
	SPI_55S	SPI	SPI_SI
	SPI_55S	SPI	SPI_A_SI_R 6 43 49
	SPI_55S	SPI	SPI_B_SI_R
SPI_SO	SPI_55S	SPI	SPI_SO 6 24 43 49
	SPI_55S	SPI	SPI_A_SO_R 6 49
	SPI_55S	SPI	SPI_B_SO
	SPI_55S	SPI	SPI_B_SO_R
SPI_CE_L0	SPI_55S	SPI	SPI_CE_R_L<0> 6 24 49
	SPI_55S	SPI	SPI_CE_L<0> 6 43 49
SPI_CE_L1	SPI_55S	SPI	SPI_CE_R_L<1> 6 24 43
	SPI_55S	SPI	SPI_CE_L<1>

SB Constraints (1 of 2)

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?
PCIE_R2D	*	=PCIE	?
PCIE_D2R	*	=PCIE	?
PCIE_9MIL	*	0.228 MM	?
PCIE_12MIL	*	0.300 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_R2D	PCIE_R2D	*	PCIE_9MIL
PCIE_D2R	PCIE_D2R	*	PCIE_9MIL
PCIE_D2R	PCIE_R2D	*	PCIE_12MIL

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Platform LAN (Nineveh) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LAN_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
GLAN_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_CLK	*	=2.5:1_SPACING	?
ENET_GLAN	*	20 MILS	?
ENET_LAN	*	=1.5:1_SPACING	?
ENET_MDI	*	25 MILS	?

DG says 30 mils min separation.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Controller Link (AMT) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLINK_12MIL	*	=STANDARD	12 MILS	5 MILS	300 MILS	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLINK	*	=1.8:1_SPACING	?
CLINK_VREF	*	12 MILS	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
PCI_AD	PCI_55S	PCI	PCI_AD<18..0> 9 24
PCI_AD19	PCI_55S	PCI	PCI_AD<19> 9 24
PCI_AD20	PCI_55S	PCI	PCI_AD<20> 9 24
PCI_AD	PCI_55S	PCI	PCI_AD<31..21> 9 24
PCI_AD	PCI_55S	PCI	PCI_PAR 9 24
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0> 9 24
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L 6 24
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L 6 24
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L 6 24
PCI_LOCK_L	PCI_55S	PCI	PCI_LOCK_L 6 24
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L 6 24
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L 6 24
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L 6 24
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L 6 24
PCI_FW_REQ_L	PCI_55S	PCI	PCI_FW_REQ_L 6 24
PCI_FW_GNT_L	PCI_55S	PCI	PCI_FW_GNT_L 6 24
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L 6 24
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L
PCI_REQ2_L	PCI_55S	PCI	PCI_REQ2_L 6 24
PCI_GNT2_L	PCI_55S	PCI	PCI_GNT2_L
INT_PIRQA_L	PCI_55S	PCI	INT_PIRQA_L 6 24
INT_PIRQB_L	PCI_55S	PCI	INT_PIRQB_L 6 24
INT_PIRQC_L	PCI_55S	PCI	INT_PIRQC_L 6 24
INT_PIRQD_L	PCI_55S	PCI	INT_PIRQD_L 6 24
INT_PIRQE_L	PCI_55S	PCI	INT_PIRQE_L 6 24
INT_PIRQF_L	PCI_55S	PCI	INT_PIRQF_L 6 24
PCIE_A_R2D	PCIE_100D	PCIE_R2D	PCIE_A_R2D_C_P
	PCIE_100D	PCIE_R2D	PCIE_A_R2D_C_N
PCIE_A_D2R	PCIE_100D	PCIE_D2R	PCIE_A_D2R_P
	PCIE_100D	PCIE_D2R	PCIE_A_D2R_N
PCIE_B_R2D	PCIE_100D	PCIE_R2D	PCIE_B_R2D_C_P
	PCIE_100D	PCIE_R2D	PCIE_B_R2D_C_N
PCIE_B_D2R	PCIE_100D	PCIE_D2R	PCIE_B_D2R_P
	PCIE_100D	PCIE_D2R	PCIE_B_D2R_N
			PCIE_EXCARD_R2D_C_P
			PCIE_EXCARD_R2D_C_N
			PCIE_EXCARD_D2R_P
			PCIE_EXCARD_D2R_N
			PCIE_FW_R2D_C_P
			PCIE_FW_R2D_C_N
			PCIE_FW_D2R_P
			PCIE_FW_D2R_N
PCIE_MINI_R2D	PCIE_100D	PCIE_R2D	PCIE_MINI_R2D_C_P 24 36
	PCIE_100D	PCIE_R2D	PCIE_MINI_R2D_C_N 24 36
PCIE_MINI_D2R	PCIE_100D	PCIE_D2R	PCIE_MINI_D2R_P 24 36
	PCIE_100D	PCIE_D2R	PCIE_MINI_D2R_N 24 36
			PCIE_ENET_R2D_C_P
			PCIE_ENET_R2D_C_N
			PCIE_ENET_D2R_P
			PCIE_ENET_D2R_N
GLAN_COMP			GLAN_COMP 6 23
ENET_KRIAS			NINEVEH_KBIAS_P
ENET_RBIAS			NINEVEH_RBIAS
(PCIE_ENET_R2D)	GLAN_100D	ENET_GLAN	ENET_GLAN_R2D_P
	GLAN_100D	ENET_GLAN	ENET_GLAN_R2D_N
(PCIE_ENET_D2R)	GLAN_100D	ENET_GLAN	ENET_GLAN_D2R_C_P
	GLAN_100D	ENET_GLAN	ENET_GLAN_D2R_C_N
ENET_LAN	LAN_55S	ENET_LAN	LAN_RSTSYNC
ENET_LAN	LAN_55S	ENET_LAN	LAN_R2D<2..0>
ENET_LAN	LAN_55S	ENET_LAN	LAN_D2R<2..0>
ENET_GLAN_CLK	LAN_55S	ENET_CLK	ENET_GLAN_CLK_R
	LAN_55S	ENET_CLK	ENET_GLAN_CLK
ENET_MDI0	ENET_100D	ENET_MDI	ENET_MDI_P<0>
	ENET_100D	ENET_MDI	ENET_MDI_N<0>
ENET_MDI1	ENET_100D	ENET_MDI	ENET_MDI_P<1>
	ENET_100D	ENET_MDI	ENET_MDI_N<1>
ENET_MDI2	ENET_100D	ENET_MDI	ENET_MDI_P<2>
	ENET_100D	ENET_MDI	ENET_MDI_N<2>
ENET_MDI3	ENET_100D	ENET_MDI	ENET_MDI_P<3>
	ENET_100D	ENET_MDI	ENET_MDI_N<3>
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_CLK 6 16 25
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_DATA 6 16 25
CLINK_NB_RESET_L	CLINK_55S	CLINK	CLINK_NB_RESET_L 6 16 25
CLINK_WLAN	CLINK_55S	CLINK	CLINK_WLAN_CLK
CLINK_WLAN	CLINK_55S	CLINK	CLINK_WLAN_DATA
CLINK_WLAN_RESET_L	CLINK_55S	CLINK	CLINK_WLAN_RESET_L
NB_CLINK_VREF	CLINK_12MIL	CLINK_VREF	NB_CLINK_VREF 6 16
SB_CLINK_VREF0	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF0 6 25
SB_CLINK_VREF1	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF1 6 25

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Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	PWR	*	BUS2PWR_GND
CLK_FSB	GND	*	BUS2PWR_GND
CLK_PCIE	PWR	*	BUS2PWR_GND
CLK_PCIE	GND	*	BUS2PWR_GND
CLK_MED	PWR	*	BUS2PWR_GND
CLK_MED	GND	*	BUS2PWR_GND

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
CK505_CPU	CLK_FSB_100D	CLK_FSB	CK505_CPU0_P	29 30
CK505_CPU	CLK_FSB_100D	CLK_FSB	CK505_CPU0_N	29 30
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_P	29 30
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_N	29 30
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_P	29 30
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_N	29 30
CK505_PCIF0	CLK_MED_55S	CLK_MED	CK505_PCIF0_CLK_ITPEN	
CK505_PCIF1	CLK_MED_55S	CLK_MED	CK505_PCIF1_CLK	6 29 30
CK505_PCI1	CLK_MED_55S	CLK_MED	CK505_PCI1_CLK	
CK505_PCI2	CLK_MED_55S	CLK_MED	CK505_PCI2_CLK	
CK505_PCI3	CLK_MED_55S	CLK_MED	CK505_PCI3_CLK	6 29 30
CK505_PCI4	CLK_MED_55S	CLK_MED	CK505_PCI4_CLK	
CK505_PCI5	CLK_MED_55S	CLK_MED	CK505_PCI5_CLK_FCTSEL	
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_48M_FSA	
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_REF0_FSC	
CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_N	29 30
CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_N	29 30
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_P	
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_N	
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_N	29 30
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_P	
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_N	
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_P	
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_N	
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_N	29 30
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_N	29 30
CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_P	
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_N	
CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_P	
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_N	
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	6 10 30
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	6 10 30
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_P	6 14 30
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_N	6 14 30
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	6 7 13 30 66
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	6 7 13 30 66
(CK505_PCIF0)	CLK_MED_55S	CLK_MED	PCI_CLK33M_LPCPLUS	6 30 43
(CK505_PCIF1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SB	6 24 30
(CK505_PCI1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_FW	
(CK505_PCI2)	CLK_MED_55S	CLK_MED	PCI_CLK33M_TPM	
(CK505_PCI3)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SMC	6 30 41
			CK505 PCI4 is project-specific	
			CK505 PCI5 is project-specific	
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	SB_CLK48M_USBCTLR	6 25 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	SB_CLK14P3M_TIMER	6 25 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_FSA	6 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_FSC	6 30
(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_P	6 9 30
(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_N	6 9 30
(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_P	6 9 30
(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_N	6 9 30
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P	
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N	
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_P	6 24 30
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_N	6 24 30
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	
(CK505_SRC4)	SATA_100D	GND	SB_CLK100M_SATA_P	
(CK505_SRC4)	SATA_100D	GND	SB_CLK100M_SATA_N	
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_P	6 16 30
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_N	6 16 30
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	6 30 36
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	6 30 36
			CK505 SRC7 is project-specific	
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P	
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N	

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
SMBUS_SMC_A_S3_SCL	SMB_5S	SMB	SMBUS_SMC_A_S3_SCL	6 44
SMBUS_SMC_A_S3_SDA	SMB_5S	SMB	SMBUS_SMC_A_S3_SDA	6 44
SMBUS_SMC_B_S0_SCL	SMB_5S	SMB	SMBUS_SMC_B_S0_SCL	
SMBUS_SMC_B_S0_SDA	SMB_5S	SMB	SMBUS_SMC_B_S0_SDA	
SMBUS_SMC_0_S0_SCL	SMB_5S	SMB	SMBUS_SMC_0_S0_SCL	6 7 44
SMBUS_SMC_0_S0_SDA	SMB_5S	SMB	SMBUS_SMC_0_S0_SDA	6 7 44
SMBUS_SMC_BSA_SCL	SMB_5S	SMB	SMBUS_SMC_BSA_SCL	6 7 44
SMBUS_SMC_BSA_SDA	SMB_5S	SMB	SMBUS_SMC_BSA_SDA	6 7 44
SMBUS_SMC_MGMT_SCL	SMB_5S	SMB	SMBUS_SMC_MGMT_SCL	6 44
SMBUS_SMC_MGMT_SDA	SMB_5S	SMB	SMBUS_SMC_MGMT_SDA	6 44

Clock & SMC Constraints

SYNC_MASTER=T9 SYNC_DATE=01/30/2007

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1	PPBUS_G3H	NET_SPACING_TYPE=PWR 6 7 8
2	PPBUS_R_G3H	NET_SPACING_TYPE=PWR 6 7 8
3	PPDCIN_G3H	NET_SPACING_TYPE=PWR 6 7 8
4	PPDCIN_G3H_R	NET_SPACING_TYPE=PWR 6 50
5	PPVBATT_G3H_R	NET_SPACING_TYPE=PWR 6 50
6	PPVBAT_G3H_CHGR_OUT	NET_SPACING_TYPE=PWR 6 59
7	PPVBAT_G3H_CHGR_REG	NET_SPACING_TYPE=PWR 6 59
8	PPVBAT_G3H_CHRGR_REG_R	NET_SPACING_TYPE=PWR 6 59
10	PPVBAT_G3H_CHRGR_REG_0	NET_SPACING_TYPE=PWR 6 59
9	PPVCORE_S0_CPU	NET_SPACING_TYPE=PWR 6 7 8
12	PPVCORE_S0_NB_GFX	NET_SPACING_TYPE=PWR 6 7 8
11	PPVDCIN_G3H_PRE	NET_SPACING_TYPE=PWR 6 45 59
13	PPVDCIN_G3H_PRE_R	NET_SPACING_TYPE=PWR 6 59
14	PPVDCIN_G3H_PRE_0	NET_SPACING_TYPE=PWR 6 59
16	PPVDCIN_G3H_PRE2	NET_SPACING_TYPE=PWR 6 59
15	PPVIN_S5_IMVP6_VIN	NET_SPACING_TYPE=PWR 6 52
18	PPVOUT_S0_LCDBKLT	NET_SPACING_TYPE=PWR 6 7 60 64
17	PPVOUT_S0_LCDBKLT_SW	NET_SPACING_TYPE=PWR 6 64
19	PP0V9_S0	NET_SPACING_TYPE=PWR 6 7 8
21	PP0V9_S3	NET_SPACING_TYPE=PWR 6 8
20	PP1V5_S0	NET_SPACING_TYPE=PWR 6 7 8
23	PP1V5_S0_NB_QDAC	NET_SPACING_TYPE=PWR 6 22
160	PP1V5_S0_NB_VCCD_CRT	NET_SPACING_TYPE=PWR 6 22
161	PP1V5_S0_NB_VCCD_QDAC	NET_SPACING_TYPE=PWR 6 19 22
22	PP1V5_S0_NB_VCCDMIPLL	NET_SPACING_TYPE=PWR
24	PP1V5_S0_NB_VCCDMIPLL_F	NET_SPACING_TYPE=PWR
25	PP1V5_S0_SB_VCCDMIPLL	NET_SPACING_TYPE=PWR 6 26 27
26	PP1V5_S0_SB_VCCDMIPLL_F	NET_SPACING_TYPE=PWR 6 27
28	PP1V5_S0_SB_VCCSATAPLL	NET_SPACING_TYPE=PWR 6 26 27
27	PP1V5_S0_SB_VCC1_5_B	NET_SPACING_TYPE=PWR 6 23 24 26 27
30	PP1V8_S0	NET_SPACING_TYPE=PWR 6 7 8
29	PP1V8_S0_ANALOG_SDVO_F	NET_SPACING_TYPE=PWR 6 61
31	PP1V8_S0_ANALOG_TMDS_F	NET_SPACING_TYPE=PWR 6 61
33	PP1V8_S0_NB_VCCTXLVDS	NET_SPACING_TYPE=PWR 6 19 22
32	PP1V8_S0_PVCC1_TMDS_F	NET_SPACING_TYPE=PWR 6 61
35	PP1V8_S0_PVCC2_TMDS_F	NET_SPACING_TYPE=PWR 6 61
34	PP1V8_S0_TMDS_F	NET_SPACING_TYPE=PWR 6 61
36	PP1V8_S3	6 7 8
38	PP1V8_S3M_NB_VCCSMCK	NET_SPACING_TYPE=PWR 6 19 21
37	PP1V8_S3_NB_VCCSMCK_RC	NET_SPACING_TYPE=PWR 6 21
39	PP1V05_S0	NET_SPACING_TYPE=PWR 6 7 8
41	PP1V05_S0_NB_VCCPEG	NET_SPACING_TYPE=PWR 6 15 19 21
140	PP1V25_S0	NET_SPACING_TYPE=PWR 6 7 8
143	PP1V25_S0M_NB_VCCA_HPLL	NET_SPACING_TYPE=PWR 6 19 21
142	PP1V25_S0_NB_DPLL	NET_SPACING_TYPE=PWR 6 22
144	PP1V25_S0_NB_PEGPLL	NET_SPACING_TYPE=PWR 6 19 21
146	PP1V25_S0_NB_PEGPLL_RC	NET_SPACING_TYPE=PWR 6 21
145	PP1V25_S0_NB_VCCA_DPLLA	NET_SPACING_TYPE=PWR 6 19 22
148	PP1V25_S0_NB_VCCA_DPLLB	NET_SPACING_TYPE=PWR 6 19 22
147	PP3V3_LCDVDD_SW	NET_SPACING_TYPE=PWR 6 60
149	PP3V3_LCDVDD_SW_F	NET_SPACING_TYPE=PWR 6 7 60
150	PP3V3_S0	NET_SPACING_TYPE=PWR 7
152	PP3V3_S0_ANALOG_SDVO_F	NET_SPACING_TYPE=PWR 6 61
151	PP3V3_S0_CK505_VDDA	NET_SPACING_TYPE=PWR 6
154	PP3V3_S0_CK505_VDDA_R	NET_SPACING_TYPE=PWR 6
153	PP3V3_S0_CK505_VDD_CPU_SRC	NET_SPACING_TYPE=PWR 6 29
155	PP3V3_S0_CK505_VDD_PCI	NET_SPACING_TYPE=PWR 6
157	PP3V3_S0_CK505_VDD_REF	NET_SPACING_TYPE=PWR 6
156	PP3V3_S0_CK505_VDD48	NET_SPACING_TYPE=PWR 6
159	PP3V3_S0_IMVP6_3V3	NET_SPACING_TYPE=PWR 6 52
158	PP3V3_S0_LCD_F	NET_SPACING_TYPE=PWR 6 7 60
160	PP3V3_S0_NBCORE_FOLLOW_R	NET_SPACING_TYPE=PWR 6 21
162	PP3V3_S0_NB_CRTDAC_F	NET_SPACING_TYPE=PWR 6 22
161	PP3V3_S0_NB_TVDAC	NET_SPACING_TYPE=PWR 6 22
163	PP3V3_S0_NB_TVDAC_F	NET_SPACING_TYPE=PWR 6 22
165	PP3V3_S0_NB_TVDAC_FOLLOW	NET_SPACING_TYPE=PWR 6 22
164	PP3V3_S0_NB_VCCA_CRTDAC	NET_SPACING_TYPE=PWR 6 19 22
167	PP3V3_S0_NB_VCCA_DAC_BG	NET_SPACING_TYPE=PWR 6 19 22
166	PP3V3_S0_NB_VCCA_TVDACA	NET_SPACING_TYPE=PWR 6 19 22
168	PP3V3_S0_NB_VCCA_TVDACB	NET_SPACING_TYPE=PWR 6 19 22
170	PP3V3_S0_NB_VCCA_TVDACC	NET_SPACING_TYPE=PWR 6 19 22
169	PP3V3_S0_SPVCC_TMDS_F	NET_SPACING_TYPE=PWR 6 61
172	PP3V3_S3	NET_SPACING_TYPE=PWR 6 7 8
171	PP3V3_S3_AP_AUX	NET_SPACING_TYPE=PWR 6 7 36
173	PP3V3_S3_TOPCASE_F	NET_SPACING_TYPE=PWR
174	PP3V3_S5	NET_SPACING_TYPE=PWR 6 7 8
176	PP3V3_S5_AVREF_SMC	NET_SPACING_TYPE=PWR 6 41 42
175	PP3V3_S5_SMC_AVCC	NET_SPACING_TYPE=PWR 6 41
178	PP3V42G3H_SW	NET_SPACING_TYPE=PWR 6 57
177	PP3V42_G3H	NET_SPACING_TYPE=PWR 6 7 8
179	PP3V42_G3H_SMC_F	NET_SPACING_TYPE=PWR
181	PP3V42_G3H_SMCUSBMUX_R	NET_SPACING_TYPE=PWR 6 39
180	PP4V5_AUDIO_ANALOG	NET_SPACING_TYPE=PWR
183	PP5V_S0	NET_SPACING_TYPE=PWR 6 7 8
182	PP5V_S0_AUDIO	NET_SPACING_TYPE=PWR
184	PP5V_S0_AUDIO_AMP	NET_SPACING_TYPE=PWR
186	PP5V_S0_DVIPORT	NET_SPACING_TYPE=PWR 6 7 37 63
185	PP5V_S0_DVIPORT_D	NET_SPACING_TYPE=PWR 6 63
187	PP5V_S0_IMVP6_VDD	NET_SPACING_TYPE=PWR 6 52
189	PP5V_S0_KBDLED_F	NET_SPACING_TYPE=PWR 6 7 40
188	PP5V_S0_SB_V5REF	NET_SPACING_TYPE=PWR 6 26 27
191	PP5V_S0_TMDS_FUSE	NET_SPACING_TYPE=PWR 6 63
190	PP5V_S0_3G_F	NET_SPACING_TYPE=PWR
192	PP5V_S3	NET_SPACING_TYPE=PWR 6 7 8
194	PP5V_S3_CAMERA_F	NET_SPACING_TYPE=PWR 6 7 60
193	PP5V_S3_IR_F	NET_SPACING_TYPE=PWR
196	PP5V_S3_USB2_EXTA	NET_SPACING_TYPE=PWR 6 39
195	PP5V_S3_USB2_EXTA_F	NET_SPACING_TYPE=PWR 6 7 37 39
197	PP5V_S5	NET_SPACING_TYPE=PWR 6 7 8
198	PP5V_S5_SB_V5REF_SUS	NET_SPACING_TYPE=PWR 6 26 27
199	PP18V5_DCIN	NET_SPACING_TYPE=PWR 6 7 50
102	PP18V5_DCIN_ONEWIRE	NET_SPACING_TYPE=PWR 6 50
103	PP18V5_G3H	NET_SPACING_TYPE=PWR 6 7 8
104	PP18V5_S5_CHGR_SW_R	NET_SPACING_TYPE=PWR 6 59

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PWR	*	=STANDARD	?
BUS2PWR_GND	*	0.228 MM	?

M82 Power and Ground Nets

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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M82 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,ISL12,ISL13,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.100 MM	0.076 MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
27P4_OHM_SE	ISL2,ISL4,ISL5	Y	0.215 MM	0.215 MM			
27P4_OHM_SE	ISL10,ISL11,ISL13	Y	0.215 MM	0.215 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	TOP,BOTTOM	Y	0.290 MM	0.290 MM			
45_OHM_SE	ISL2,ISL4,ISL5	Y	0.091 MM	0.091 MM			
45_OHM_SE	ISL10,ISL11,ISL13	Y	0.091 MM	0.091 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.235 MM	0.235 MM			
50_OHM_SE	ISL2,ISL4,ISL5	Y	0.070 MM	0.070 MM			
50_OHM_SE	ISL10,ISL11,ISL13	Y	0.070 MM	0.070 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.190 MM	0.190 MM			
55_OHM_SE	ISL2,ISL4,ISL5	Y	0.070 MM	0.070 MM	55OHM SE ON INTERNAL LAYERS NOT ACHIEVABLE IN M82 STACKUP USING 50OHM SE		
55_OHM_SE	ISL10,ISL11,ISL13	Y	0.070 MM	0.070 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	TOP,BOTTOM	Y	0.310 MM	0.310 MM		0.130 MM	0.130 MM
70_OHM_DIFF	ISL2,ISL4,ISL5	Y	0.132 MM	0.132 MM		0.200 MM	0.200 MM
70_OHM_DIFF	ISL10,ISL11,ISL13	Y	0.132 MM	0.132 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	TOP,BOTTOM	Y	0.230 MM	0.230 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL2,ISL4,ISL5	Y	0.090 MM	0.090 MM		0.200 MM	0.200 MM
85_OHM_DIFF	ISL10,ISL11,ISL13	Y	0.090 MM	0.090 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
87_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
87_OHM_DIFF	TOP,BOTTOM	Y	0.220 MM	0.220 MM		0.180 MM	0.180 MM
87_OHM_DIFF	ISL2,ISL4,ISL5	Y	0.082 MM	0.082 MM		0.200 MM	0.200 MM
87_OHM_DIFF	ISL10,ISL11,ISL13	Y	0.082 MM	0.082 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	TOP,BOTTOM	Y	0.190 MM	0.190 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL2,ISL4,ISL5	Y	0.085 MM	0.085 MM		0.250 MM	0.250 MM
90_OHM_DIFF	ISL10,ISL11,ISL13	Y	0.085 MM	0.085 MM		0.250 MM	0.250 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	TOP,BOTTOM	Y	0.170 MM	0.170 MM		0.205 MM	0.205 MM
100_OHM_DIFF	ISL2,ISL4,ISL5	Y	0.065 MM	0.065 MM		0.280 MM	0.280 MM
100_OHM_DIFF	ISL10,ISL11,ISL13	Y	0.065 MM	0.065 MM		0.280 MM	0.280 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
BGA_P3MM	*	0.3 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.28:1_SPACING	*	0.228 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V8_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
NB_STATIC	*	=STANDARD	?

M82 Rule Definitions

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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